SERVICE MANUAL

ASTRO INVADER

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ASTRO INVADERS SERVICE MANUAL

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SECTION 1
INSTALLATION

1.1 INTRODUCTION

This game has been STERN final tested and is ready to play, but on all games there are some items that must be checked after shipment. Making these visual inspections may avoid time consuming service work later. Minor troubles caused by abusive handling in shipment are unavoidable, such as cable connectors that may have become loosened. Check ALL CONNECTORS on the game to make sure they are firmly seated. Check to make sure that the game control boards are firmly seated (See Figure B). Examine the exterior of the game cabinet for dents, chips or broken parts. Check all major sub-assemblies, control panel and T.V. monitor to make sure that they have not loosened up during shipment.

1.2 VISUAL INSPECTION BEFORE PLUGGING IN LINE CORD

1. Check that the primary wiring of the transformer corresponds to the location voltage (See Figure E).

2. Check the transformer for any foreign material shorting across wiring lugs.

3. Check that fuses are firmly seated and making good contact.

4. Check the T.V. for any foreign material that could cause shorts (VISUAL INSPECTION ONLY).

5. Check game boards in electronics card cage for any foreign material that could cause shorts. Make sure all circuit boards are pushed into the mother board.

1.3 ON/OFF POWER INTERLOCK SWITCHES

1. The on/off power switch is located on the top right side 12" from the front.

2. There are two interlock main power switches, one by the front door (See Figure A) and one on the back access panel (See Figure B).

3. Interlock switches interrupt all power from game except service outlet and fluorescent lights for Marquee. Interlock switches can be locked in "on" position by pulling stem out when servicing game.

1.4 GENERAL INFORMATION

1. On front door there is a service switch (See Figure A). Depressing this switch will coin machine without advancing coin counter.

2. The counter is inside the front door on the left hand side of cabinet. Counter will advance anytime coin (coins) pass through coin chute.

3. There are two coin chutes on the front door that are connected in parallel. (Note: They cannot be adjusted to work separately).

4. Game adjustment switches are located on I/O board. (See Figure C for adjustments).

5. The electronics package (card cage) used in Astro Invader is the same for stand-up model and cocktail table model. (They can be interchanged if one jumper is changed on I/O board).

6. Volume control for electronic sound is located on I/O board. (See Figure C).

7. Power supply has an adjustment for the +5 VDC regulator, this MUST BE SET BETWEEN +5.3 VDC AND +5.6 VDC. (See Figure D for test points on power supply and adjustment pot.

ASTRO INVADER

FRONT CABINET

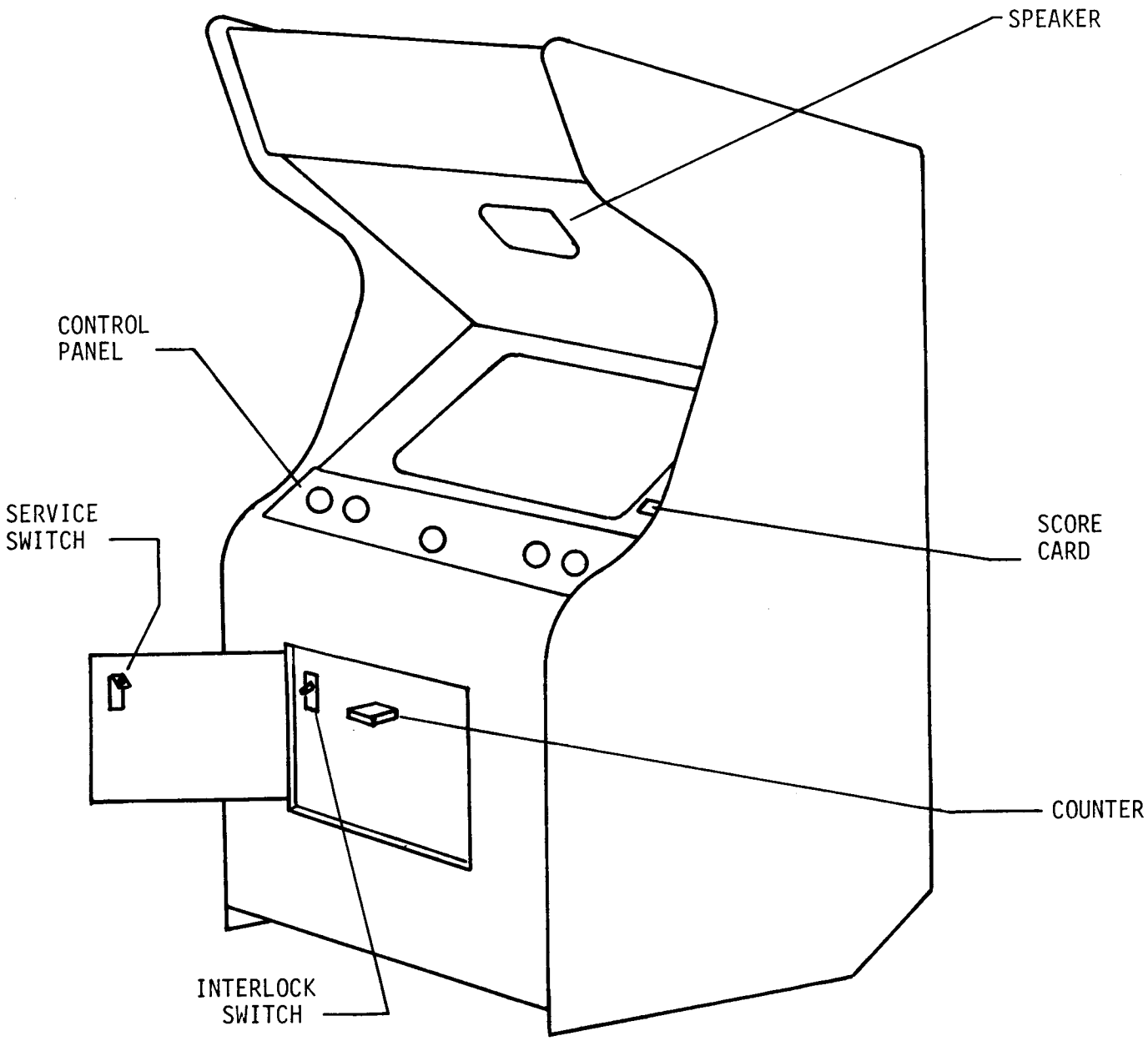


FIGURE-B

ASTRO INVADER

REAR CABINET

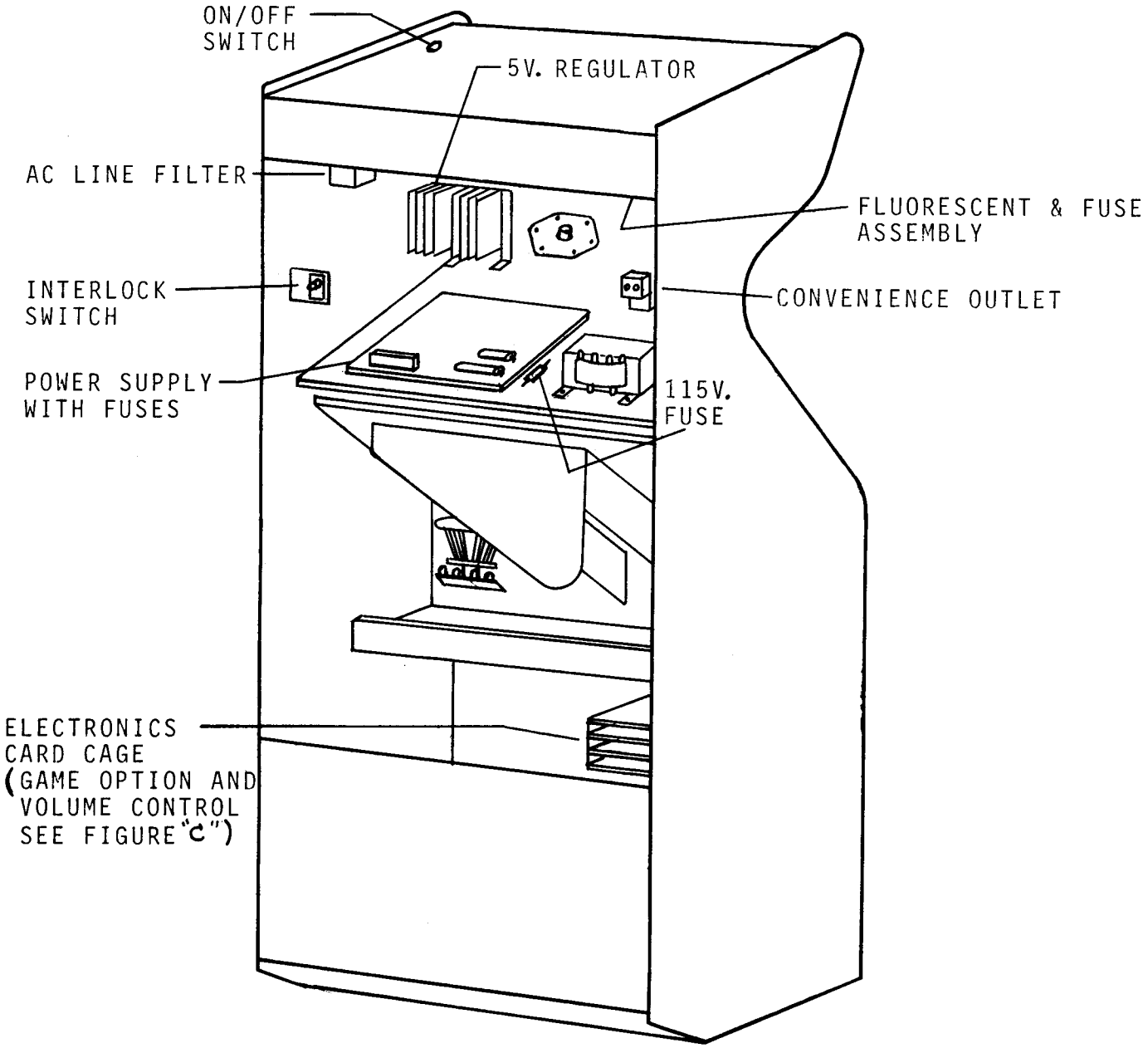
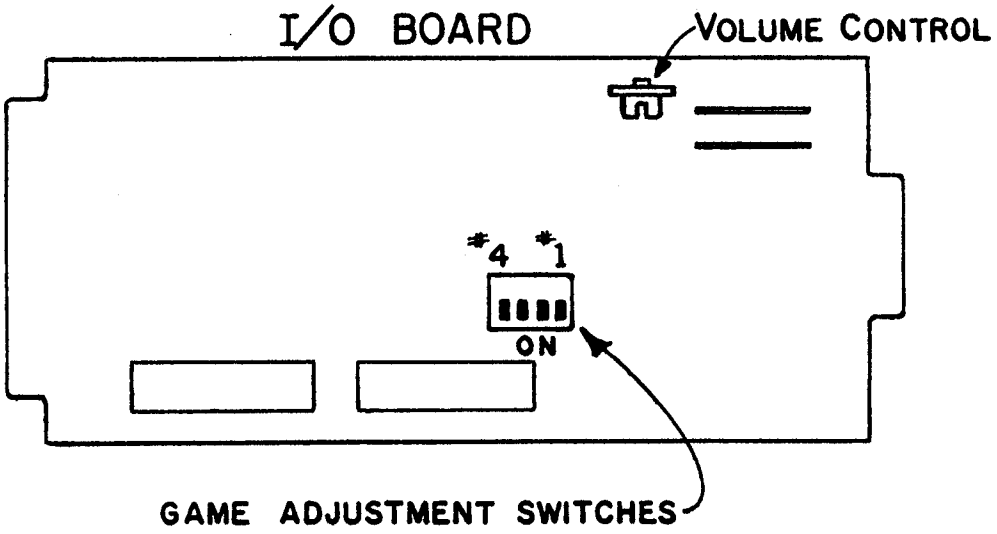
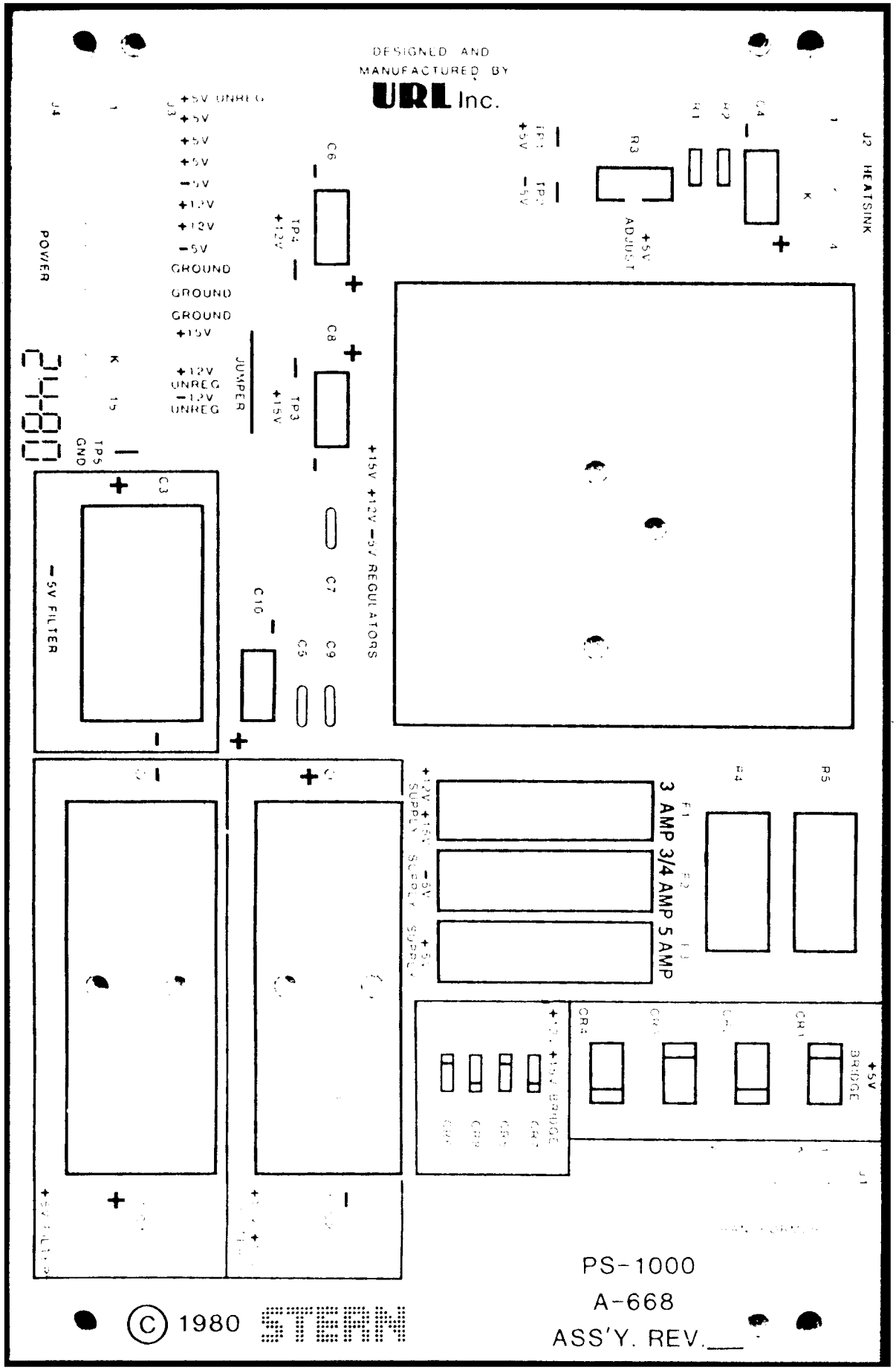


FIGURE-C

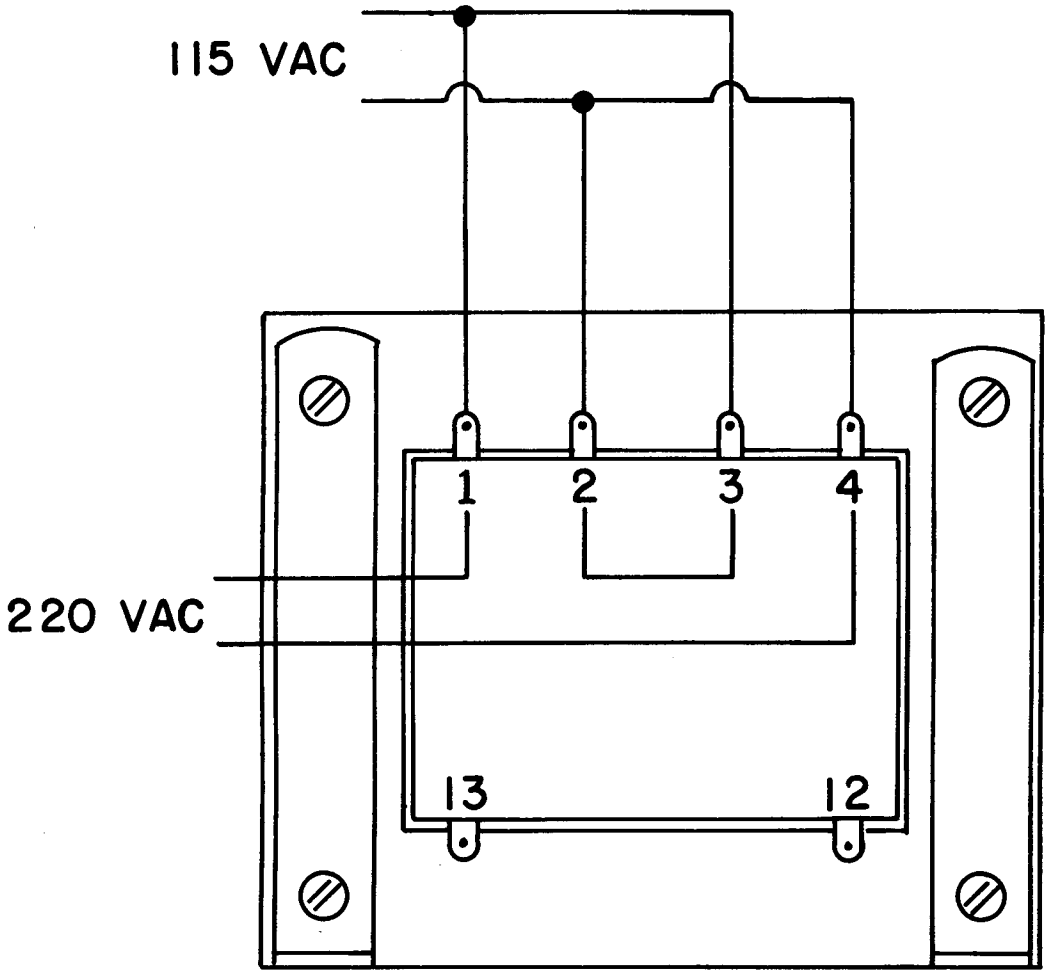
SW #1 OFF	SW #1 ON
10,000 SCORE AWARDS ADDITIONAL BASE	20,000 SCORE AWARDS ADDITIONAL BASE

OPTIONS	GAME ADJUSTMENT SWITCHES #1	#2	#3	#4
BONUS 20,000 PTS.	ON			
BONUS 10,000 PTS.	OFF			
4-DEFENSE BASES		ON		
3-DEFENSE BASES		OFF		
3-COINS-1PLAY			OFF	OFF
2-COINS-1PLAY			ON	OFF
1-COIN-2PLAYS			OFF	ON
1COIN-1PLAY			ON	ON




DESIGNED AND
MANUFACTURED BY
URL Inc.
POWER
J4
J3
+5V UNREG
+5V
+5V
+5V
-5V
+12V
+12V
-5V
GROUND
GROUND
GROUND
+15V
+12V UNREG
-12V UNREG
JUMPER
TP4 +12V
TP3 +15V
TP5 GND
TP1 +5V
TP2 -5V
R1
R2
R3
+5V ADJUST
C4
J2 HEATSINK
C6
C8
C10
C3
C7
C9
C5
-5V FILTER
+15V +12V -5V REGULATORS
F1
F2
F3
3 AMP 3/4 AMP 5 AMP
R4
R5
+12V +15V SUPPLY
-5V SUPPLY
+5V SUPPLY
CR4
CR3
CR2
CR1
+5V BRIDGE
+12, +15V BRIDGE
J1
PS-1000
A-668
ASS'Y. REV.___
© 1980 STEAM

TRANSFORMER



STERN 16D-10

SECTION 2
BASIC LOGIC FUNCTIONS

2.1 HEXADECIMAL NUMBERING SYSTEM

Any digital device inherently has two stable states, on or off. Relays are inherently digital, as are switches. An "on" device is usually defined as being at a logical one. An "off" device is at a logical zero. It follows naturally that the binary numbering system is perfect to describe digital systems, since it has two possible states, 0 and 1.

Basic rules for binary additions follow:

	(a)	(b)	(c)	(d)
	0_2	1_2	1_2	1_2
Plus	$+1_2$	$+0_2$	$+0_2$	$+1_2$
Sum	1_2	1_2	1_2	10_2

The subscript above indicates that the base of the numbering system is 2. Notice that in example (d), the sum overflowed the base of the numbering system, so a carry was generated into the next most significant digit position. The same thing happens in the decimal numbering system when 1 is added to 9.

		OR	
	9_{10}		99_{10}
Plus	$+1_{10}$		$+\ 1_{10}$
	10_{10}		100_{10}

It is convenient to refer to numbers in the binary system as digits but problems are encountered when the number 9 is exceeded. Therefore, letters were assigned to numbering system:

BINARY	HEXADECIMAL
0000_2	0_H
0001_2	1_H
0010_2	2_H
0011_2	3_H
0100_2	4_H
0101_2	5_H
0110_2	6_H
0111_2	7_H
1000_2	8_H
1001_2	9_H
1010_2	A_H
1011_2	B_H
1100_2	C_H
1101_2	D_H
1110_2	E_H
1111_2	F_H

Note that the subscript H is used to denote the hexadecimal number rather than 16, to eliminate confusion. A hexadecimal digit occupies 4 bits, or binary digits, and is sometimes referred to as a nibble. Two nibbles or eight bits equals one byte. The remainder of this manual will deal with bytes and hexadecimal numbers. One final point: What happens when 1H is added to FH?

$$\begin{array}{lll} & F_H & \\ \text{Plus} & +1_H & \\ \hline \text{Sum} & 10_H & \text{OF COURSE!} \end{array}$$

2.2 LOGIC UNITS OF SYSTEM

The logic units used in this manual are illustrated and described in Table 2-1.

Table 2-1 Basic Logic Units

NOTE: When referring to the Truth Tables, use the following definitions.

1	logical one, greater than +2.4 volts
0	logical zero, less than +0.8 volts
X	don't care, either one or zero
HI - Z	off, neither a one or a zero
↑	a zero to one transistion
↓	a one to zero transition
Qn*	the state of the output at the last active transition of the clock or clear.

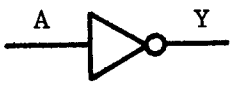
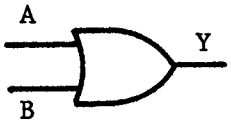
FUNCTION	SYMBOL	TRUTH TABLE
NOT		A | Y 0 | 1 1 | 0
BUFFER		A | Y 0 | 0 1 | 1
OR		A | B | Y 0 | 0 | 0 0 | 1 | 1 1 | 0 | 1 1 | 1 | 1

Table 2-1 Basic Logic Unit (Cont'd)

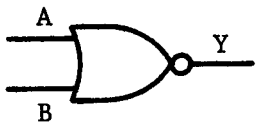
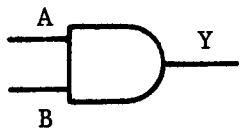
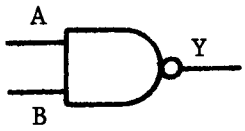
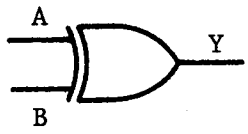
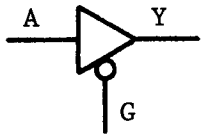
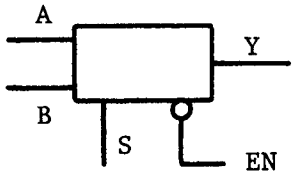
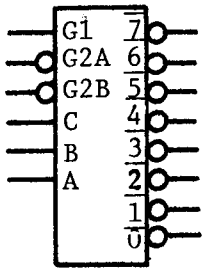
FUNCTION	SYMBOL	TRUTH TABLE
NOR		A B Y 0 0 1 0 1 0 1 0 0 1 1 0
AND		A B Y 0 0 0 0 1 0 1 0 0 1 1 1
NAND		A B Y 0 0 1 0 1 1 1 0 1 1 1 0
EXCLUSIVE OR		A B Y 0 0 0 0 1 1 1 0 1 1 1 0
TRI-STATE BUFFER		A G Y 0 0 0 1 0 1 0 1 HI-Z 1 1 HI-Z
TWO-INPUT MULTIPLEXER		A B S EN Y X X X 1 0 0 X 0 0 0 1 X 0 0 1 X 0 1 0 0 X 1 1 0 1

Table 2-1 Basic Logic Unit (Cont'd)

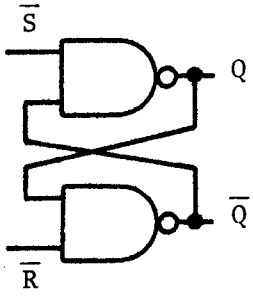
FUNCTION | SYMBOL | TRUTH TABLE

3 LINE TO
8 LINE DECODER



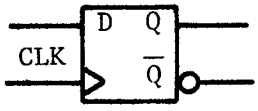
G1	G2A	G2B	C	B	A	$\overline{7}$	$\overline{6}$	$\overline{5}$	$\overline{4}$	$\overline{3}$	$\overline{2}$	$\overline{1}$	$\overline{0}$
0	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	1	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

$\overline{S}$ $\overline{R}$
FLIP FLOP



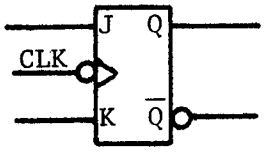
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	Qn	$\overline{Qn}$

D TYPE
FLIP FLOP



D	CLK	Q	$\overline{Q}$
X	1	Qn	$\overline{Qn}$
X	0	Qn	$\overline{Qn}$
1	↑	1	0
0	↑	0	1

J - K TYPE
FLIP FLOP



J	K	CLK	CLR	Q	$\overline{Q}$
X	X	X	0	0	1
X	X	0	1	Qn	$\overline{Qn}$
X	X	1	1	Qn	$\overline{Qn}$
0	0	↓	1	Qn	$\overline{Qn}$
0	1	↓	1	0	1
1	0	↓	1	1	0
1	1	↓	1	$\overline{Qn}$	Qn

SECTION 3
GAME THEORY OF OPERATION

3.1 GENERAL

NOTES: Signals referred to in the following discussion will occasionally have an asterisk (*) following the signal name. The asterisk denotes a negative true, or true on logical zero signal.

Astro Invaders is a color, Z-80 microprocessor based video game. The basic video technique utilized is that of the Mass RAM Buffer in which an individual bit of Random Access Memory (RAM) is reserved for each possible spot, or picture element (PIXEL) on the screen. There are 224 horizontal lines displayed on the monitor with each line containing 256 pixels for a total of 56,244 possible spots to be accessed from RAM. In addition to the pixel display, the screen is divided into 896 8-pixel by 8-pixel color boxes. Any one of eight colors can be displayed in any of the boxes. The system also includes special circuits which can invert, or flip the picture under the control of the microprocessor. The flip feature is utilized only in the cocktail version of the Astro-Invaders game.

3.2 SYSTEM BLOCK DIAGRAM DESCRIPTION

As shown in Figure 3-1, the game is essentially comprised of three main printed circuit (p.c.) boards, (Processor Board, Video Board and I/O Sound Board) all of which plug into a mother board.

The Processor Board provides the control functions and contains the microprocessor, data and address bus buffers, RAM and PROM. The game program is contained in the PROM. Also, a clock oscillator is provided to generate the CPU clock.

The Video Board contains the Mass Ram Buffer, horizontal and vertical address counters for the RAM, Sync Generation circuitry and the color look-up circuitry.

The I/O Sound Board contains all the sound generators, the audio amplifier, the input circuitry for player controls, coin-switch and game setting switches. The driver for the coin counter is also on this board.

The remaining sections of the system consist of the monitor, the power supply, cabinet, controls and cabling.

3.3 PROCESSOR BOARD BLOCK DIAGRAM DESCRIPTION

The control portion of the Processor Board is the Z-80 microprocessor (See Figure 3-2). A two megahertz crystal controlled oscillator circuit generates the processor clock. The Address and Data Busses are both buffered to provide adequate drive for the external circuitry. Normally, these buffers would be disabled by CPU BUSACK* signal. However, this signal is not used in the Astro Invaders game.

The game program is contained in PROMS 1 thru 7, (Type 2708 PROMS). Scratch Pad RAM is used for temporary storage by the processor. A three-line to eight-line decoder selects the PROM and RAM. Other signals that are buffered are: (1) Processor RFSH* (a signal generated by the Z-80 to refresh the dynamic RAM's), (2) IORQ* (the processor brings this signal true to execute an Input/Output operation). IORQ* is also gated with RD* (the processor is doing a read operation) and WR* (the processor is doing a write operation) to form IORD* and IOWR* (signifying that the processor is doing an Input or an Output operation, respectively). The signals MREQ* (the processor is doing a memory operation) and WR* (the processor is writing), are also buffered. These signals, along with the data and address busses are connected to the mother board and hence to the other boards.

The mother board distributes the three voltages - +5, -5 and +12. The +5 volt supply goes to all the chips while +12 and -5 volts are required only by the PROMS.

Two signals, WAIT* (the processor is waiting for an external event to happen) and INTERRUPT* (the processor is signaled to stop normal program execution, and do something spcial) are received from the video board. The RESET signal is received from the mother board to start program execution from a known place (0000h for the Z-80).

3.4 I/O SOUND BOARD BLOCK DIAGRAM DESCRIPTION

For the sound board discussion refer to Figure 3-3. The board consists primarily of two Peripheral Interface Adapter (PIA) chips, one of which is used for the input and the other for the output. The Data Bus, part of the Address Bus, the Reset, the IORD* and the IOWR* all connect to both chips. The states of address lines A2 and A3 (during an I/O operation) select which PIA will be accessed. Player one and two controls for left-move, right-move and fire are brought into the I/O sound board. In the upright cabinet, the player one and two controls are used in parallel. These switches are connected to a debounce circuit which operates by discharging a capacitor through a resistor and the switch until the capacitor discharges below the threshold of a Schmitt trigger inverter. This digital signal is then input to the processor via the PIA.

The coin switch is connected to a debounce and pulse-stretching one-shot to insure that the processor will recognize the coin switch. At the same time, a transistor is turned on to advance the coin counter. A service switch is provided to add a credit but does not advance the coin counter. Four game-parameter-setting switches are also provided. Refer to the section on game set-up for details of their usage.

The second PIA is used as an output port. Most of the output bits are used to control sounds. The digital output of these sound control bits are applied to open collector buffers to turn on the various sound effects by removing a ground from the sound generating circuit. The various sound effects are generated by operational amplifier circuits connected as oscillators, amplifiers, differentiators and integrators. Resistor and capacitor values determine the frequency of the sounds. Other sounds are generated by a digital noise source, and a digital timer chip. These sounds are added together and applied to a Power Amplifier. A sound enable line (not shown in the diagram)

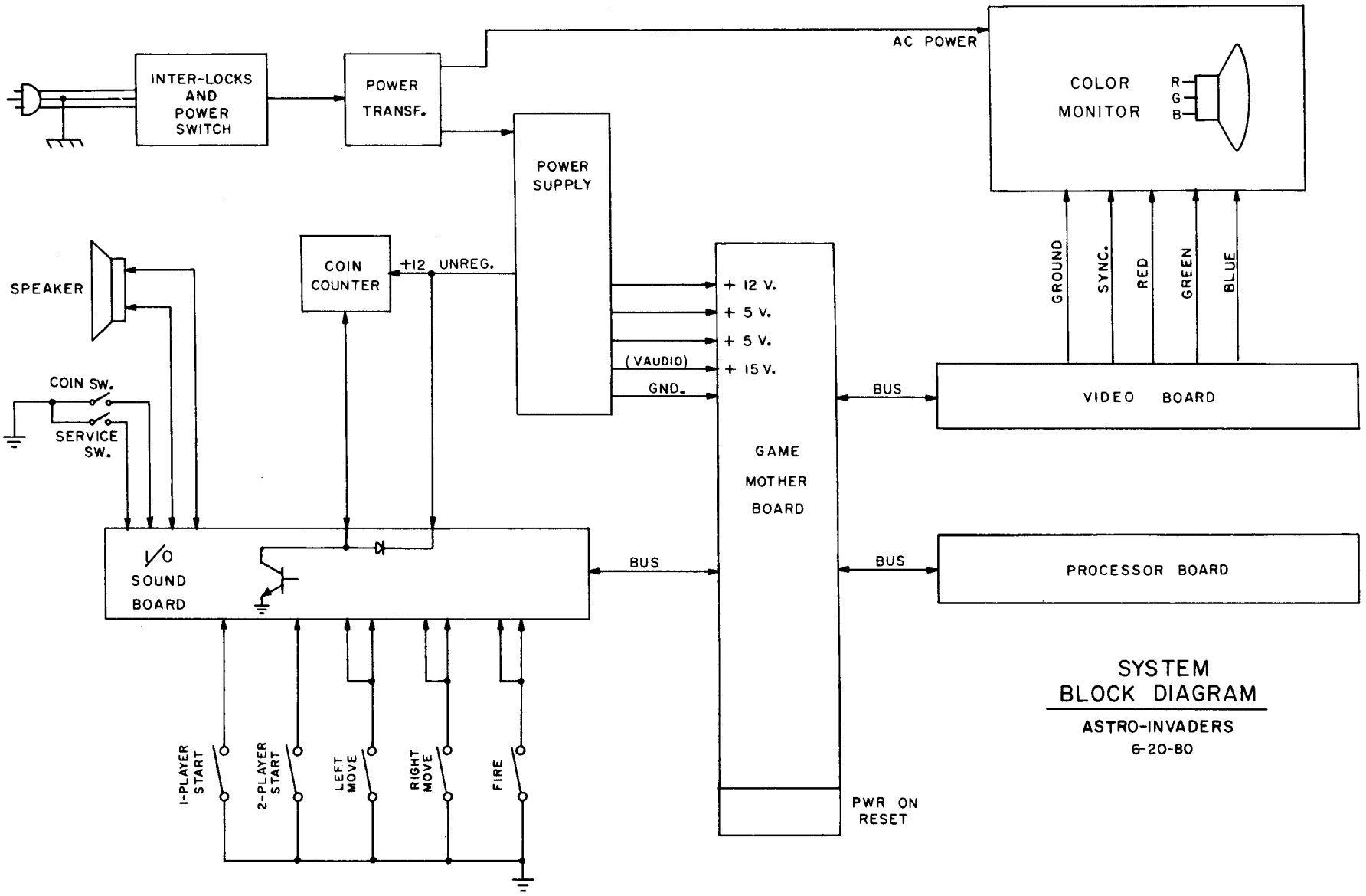

INTER-LOCKS AND POWER SWITCH
POWER TRANSF.
AC POWER
COLOR MONITOR
R
G
B
POWER SUPPLY
SPEAKER
COIN COUNTER
+12 UNREG.
GROUND
SYNC.
RED
GREEN
BLUE
+ 12 V.
+ 5 V.
+ 5 V.
(VAUDIO)
+ 15 V.
GND.
COIN SW.
SERVICE SW.
BUS
VIDEO BOARD
GAME MOTHER BOARD
I/O SOUND BOARD
BUS
BUS
PROCESSOR BOARD
1-PLAYER START
2-PLAYER START
LEFT MOVE
RIGHT MOVE
FIRE
PWR ON RESET
SYSTEM BLOCK DIAGRAM
ASTRO-INVADERS
6-20-80

FIGURE 3-1

turns the Power Amplifier on and off. The summed audio signal is applied to one side of the Power Amplifier. This audio signal is also inverted and applied to the other side of the Power Amplifier. The speaker is connected in a "bridge" configuration between the outputs of the Power Amplifier.

The output port supplies two additional outputs. One output is used to turn the monitor screen red whenever an Invader explosion contacts the player's tank, or whenever UFO reaches the bottom of the screen. The explosion sound also occurs at this time. The other output controls the video screen flip. The flip is required when the game is mounted in a cocktail table so the image will be inverted and appear correct to players on opposite sides of the table. The processor can flip the image by taking this line to a one or a zero. In the case of the Upright cabinet, the image should not be flipped. Therefore, the wire is strapped to ground to prevent the flip from occuring.

An edge connector (opposite from the Mother Board connector) is used to connect the player controls, the speaker, and the coin counter. The power supply for the board is +5 volts for the PIA's and most of the logic, +12 volts for the operational amplifiers and VAUDIO for the audio Power Amplifier.

3.5 VIDEO BOARD BLOCK DIAGRAM DESCRIPTION

The Video Board (Figure 3-4) contains sixteen 4K bit RAM's. The addresses to the RAM's are received from the Processor address data bus, and also from the vertical and horizontal address counters. The horizontal and vertical address counters cause the RAM to be read in ascending address order. The data read is then applied to a shift register and shifted through a color gating circuit to the monitor. Two video shift registers are used. One is loaded in reverse order from the other. The output data is selected by the UPRIGHT*/Flip line. If the UPRIGHT*/Flip bit is "set" (logical one), the addresses coming from the counters are inverted. The net effect of this is to cause the RAM to be read in reverse or descending order. This action in conjunction with the reverse video shift register, effectively flips the monitor picture.

The video board is driven by a 4.915 MHZ crystal controlled oscillator which is divided down by the Horizontal and Vertical Address Counters. As stated before, these counters generate Addresses to the RAMS. They also provide signals to the SYNC generating circuitry, the timing circuitry to load and clock the video shift registers, the RAM access arbitrator and the color look-up circuit. Finally, interrupts to the processor are generated by this circuit.

The RAM access arbitrator determines when the processor can have access to the RAM. If the Z-80 attempts RAM access during a video read cycle, the processor is put into a WAIT* state until the video cycle is completed. Finally, gating is provided to turn the screen red when the player loses a tank. A 10 pin connector is used to connect the video output to the color monitor.

3.6 POWER SUPPLY BLOCK DIAGRAM DESCRIPTION

The Power Supply (Figure 3-5) line cord terminates internally at the convenience outlet which is powered any time the game is plugged in. From this

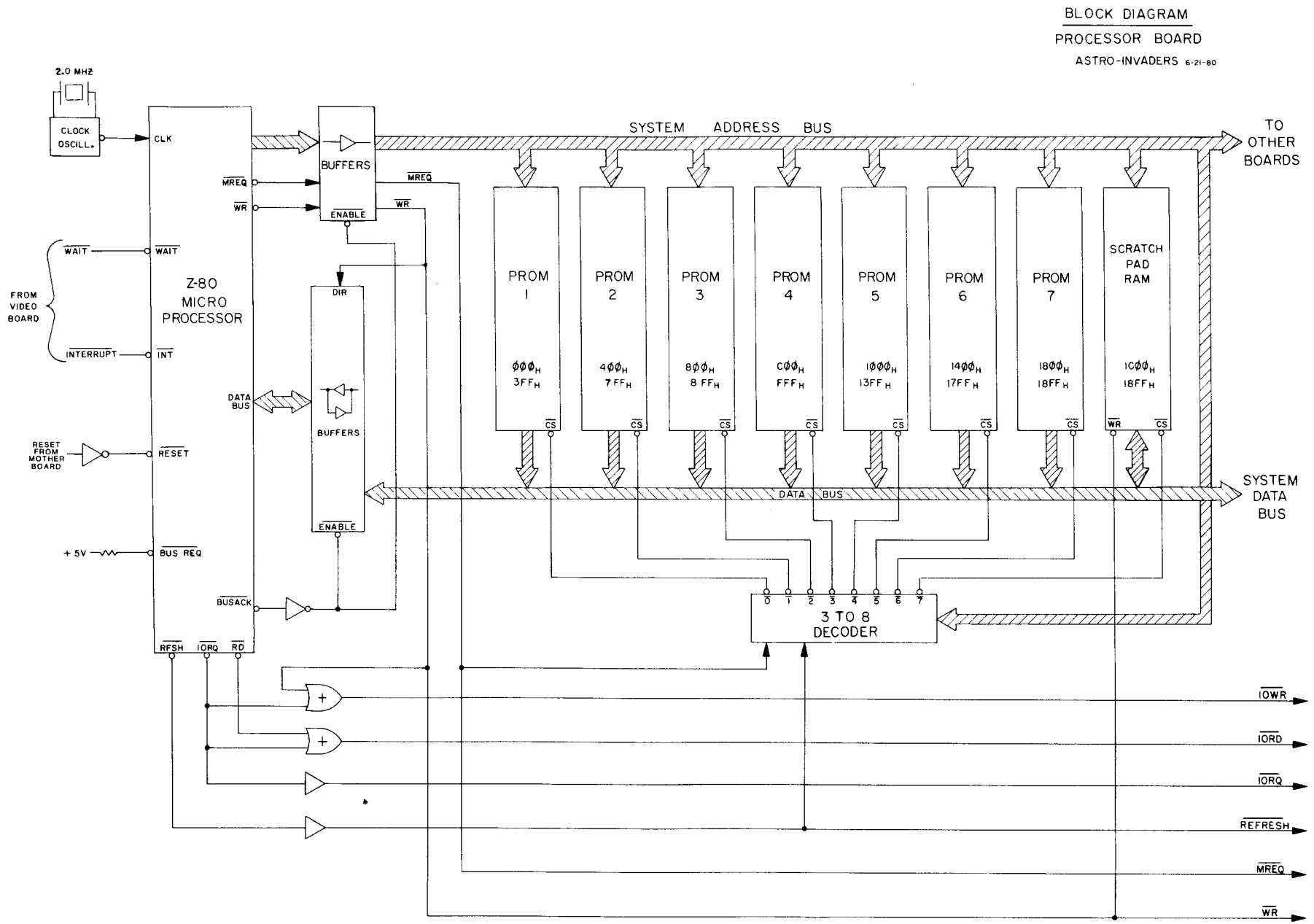

BLOCK DIAGRAM
PROCESSOR BOARD
ASTRO-INVADERS 6-21-80
2.0 MHz
CLOCK OSCILL.
CLK
Z-80 MICRO PROCESSOR
WAIT
INTERRUPT
INT
RESET
BUS REQ
BUSACK
RFSH
IORQ
RD
MREQ
WR
BUFFERS
ENABLE
DIR
DATA BUS
FROM VIDEO BOARD
RESET FROM MOTHER BOARD
+5V
SYSTEM ADDRESS BUS
TO OTHER BOARDS
PROM 1
PROM 2
PROM 3
PROM 4
PROM 5
PROM 6
PROM 7
SCRATCH PAD RAM
CS
SYSTEM DATA BUS
3 TO 8 DECODER
IOWR
IORD
IORQ
REFRESH
MREQ
WR

FIGURE 3-2

outlet power is applied through the power switch which disconnects both sides of the line. Downstream from the power switch are the line filter, and fluorescent light to illuminate the Marquee above the CRT. The load side of the line filter and varistor combination is connected to the front and rear interlock switches, which also break both sides of the line. Both switches operate identically and are electrically closed as long as the door is closed. The switch opens when the door opens, but has a manual service position to bypass the switch for power application during maintanance. From the interlock switches, power is applied to the line fuse (3A Slo-Blo for 120 Vac line, 1.5A Slo-Blo for 240 Vac line). The output of the fuse is applied to the power transformer which steps the voltage down for application to the coin door general illumination circuits, the audio supply, +12, +5 and -5 volt regulated power supplies, and an isolated winding for the color monitor. Rectifiers, filters, and regulators are mounted on the Power Supply P.C. board to regulate the voltages required for game operation. The Power Supply P.C. board has a +5 volt adjustment pot. This control should be adjusted to assure +5 volts at the game boards. Adjusting the supply for 5.3 volts at the p.c. board test point (TP1) will compensate for losses in the game cable.

The D.C. power supplies provide power for the following circuits:

+5 VOLT REG:	MOST OF THE GAME LOGIC CIRCUITRY
+12 VOLT REG:	PROM'S ON PROCESSOR BOARD OP-AMPS ON I/O SOUND BOARD. COLOR PROM ON VIDEO BOARD
+12 VOLT UNREG:	COIN COUNTER
+15 VOLT MAX:	AUDIO SUPPLY TO POWER AMPLIFIER
-5 VOLT REG:	PROMS'S ON PROCESSOR BOARD COLOR PROM ON VIDEO BOARD
+5 VOLT UNREG:	NOT USED
-5 VOLT UNREG:	NOT USED

The power transformer has a split primary that is wired in parallel for 120 Vac line, and can be wired in series for 240 Vac line.

3.7 MOTHER BOARD DESCRIPTION

The Mother Board is located at the end of the card cage and provides the electrical connectors for all boards that are inserted. The Mother Board contains four identically connected edge connectors, three of which are utilized by the three other boards while one position remains empty. Any board can be inserted into any of the four positions for ease of servicing. In addition to its interconnection function for all boards of the system, the Mother Board contains a one-shot which provides power-on reset.

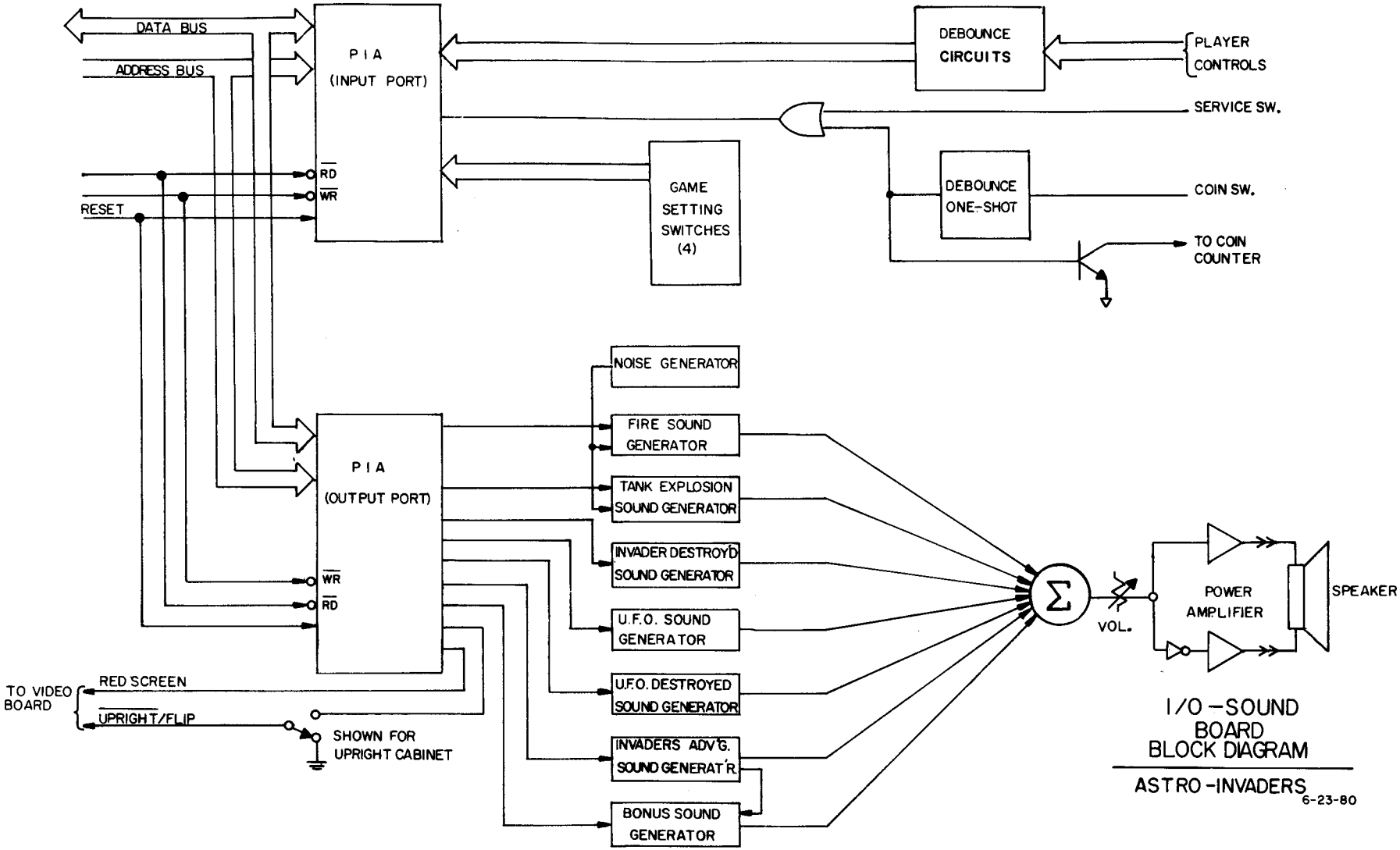

DATA BUS
ADDRESS BUS
RESET
P I A
(INPUT PORT)
RD
WR
DEBOUNCE
CIRCUITS
PLAYER
CONTROLS
SERVICE SW.
GAME
SETTING
SWITCHES
(4)
DEBOUNCE
ONE-SHOT
COIN SW.
TO COIN
COUNTER
NOISE GENERATOR
FIRE SOUND
GENERATOR
TANK EXPLOSION
SOUND GENERATOR
INVADER DESTROYD
SOUND GENERATOR
U.F.O. SOUND
GENERATOR
U.F.O. DESTROYED
SOUND GENERATOR
INVADERS ADV'G.
SOUND GENERAT'R.
BONUS SOUND
GENERATOR
P I A
(OUTPUT PORT)
WR
RD
Σ
VOL.
POWER
AMPLIFIER
SPEAKER
TO VIDEO
BOARD
RED SCREEN
UPRIGHT/FLIP
SHOWN FOR
UPRIGHT CABINET
I/O-SOUND
BOARD
BLOCK DIAGRAM
ASTRO-INVADERS
6-23-80

FIGURE 3-3

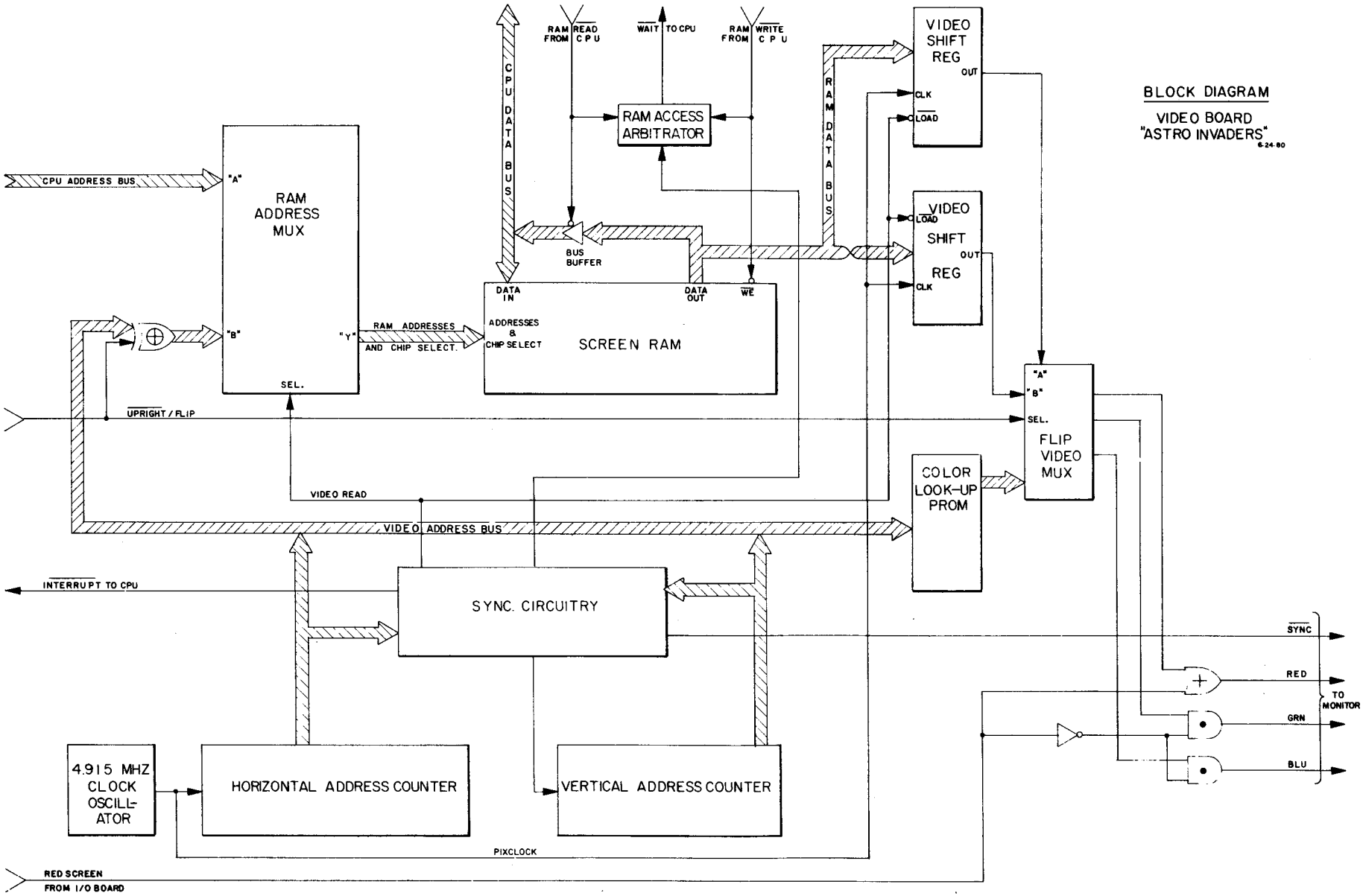
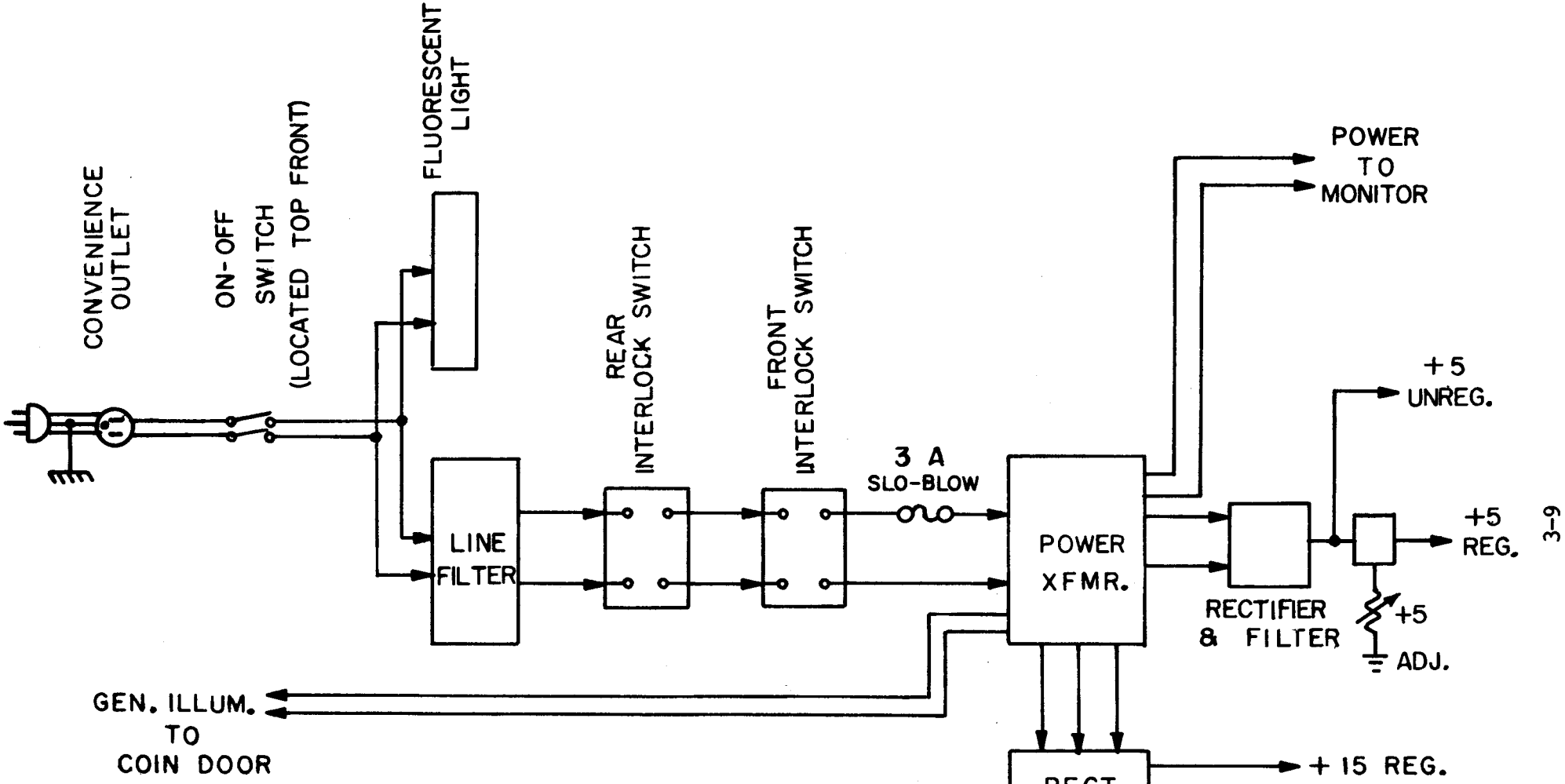

BLOCK DIAGRAM
VIDEO BOARD
"ASTRO INVADERS"
6-24-80
RAM FROM READ C P U
WAIT TO CPU
RAM FROM WRITE C P U
C P U D A T A B U S
R A M D A T A B U S
VIDEO SHIFT REG
OUT
CLK
LOAD
RAM ACCESS ARBITRATOR
CPU ADDRESS BUS
"A"
RAM ADDRESS MUX
"B"
"Y"
SEL.
BUS BUFFER
DATA IN
DATA OUT
WE
RAM ADDRESSES AND CHIP SELECT.
ADDRESSES & CHIP SELECT
SCREEN RAM
VIDEO SHIFT REG
UPRIGHT / FLIP
FLIP VIDEO MUX
COLOR LOOK-UP PROM
VIDEO READ
VIDEO ADDRESS BUS
INTERRUPT TO CPU
SYNC. CIRCUITRY
SYNC
RED
GRN
BLU
TO MONITOR
4.915 MHZ CLOCK OSCILL-ATOR
HORIZONTAL ADDRESS COUNTER
VERTICAL ADDRESS COUNTER
PIXCLOCK
RED SCREEN FROM I/O BOARD

FIGURE 3-4



BLOCK DIAGRAM

POWER SUPPLY
ASTRO INVADERS

6-25-80

FIGURE 3-5

SECTION 4
DETAILED THEORY OF OPERATION

4.1 CPU BOARD

The control portion of the CPU Board is the Z-80 microprocessor. Basically, the Z-80 performs the following functions: It fetches an instruction, or command from a program memory and then executes that instruction. Usually, the processor fetches and executes instructions in a sequential manner and it does this quite rapidly. The ability to do tasks quickly is one of the two significant features of the microprocessor. The other feature is the ability to modify the order of program execution as a result of previous conditions. This "Decision Making" ability makes it extremely versatile.

Information in the form of instructions and data is contained in a "Program Memory" built up of seven type 2708 PROM's (refer to the CPU Schematic Diagram). These PROM's are addressed by the Z-80's Address Bus. The information addressed is then applied to the Data Bus and input back to the Z-80 for processing. Occasionally, the Z-80 will have to store information in a temporary location and it uses the "Scratch Pad" RAM for this. Actually, there are two groups of RAM in the system, the Scratch Pad previously mentioned, and a Video RAM. The Video RAM will be discussed in a later section. For the present, it can be stated that both RAM's appear identical to the Z-80, except that they occupy different addresses.

Occasionally, the Z-80 has to access information outside of its normal sphere of influence such as the RAM's and PROM's. These "Outside World" events (coin switch closures, player movements, etc.) have to be acted upon. Also, the processor has to affect the "Outside World", such as flipping the picture or advancing the coin counter or turning on sounds at the appropriate time. These Input/Output (I/O) functions are treated differently than the normal Z-80 instructions. Any time the Z-80 attempts to access memory-whether to read a command (OPCODE FETCH) or to read a previously stored byte of data (MEMORY READ) or to store a data byte (MEMORY WRITE)-it brings its (MREQ*) pin true (a logical zero). On diagrams, a bar over the pin name implies that the function is true, or assertive, when it is at a logical zero. In the text, an asterisk replaces the bar (NOT function). The direction of data flow is signified by the RD* and WR* pins. An RD* implies that the processor is reading data and that the data is flowing from the addressed device to the processor. A WR* implies that the processor is writing data and that the data is flowing from the processor to the addressed device. When the processor is accessing a peripheral or Input/Output device, it asserts (brings true) its IORQ* (Input/Output Request) pin. A brief description of the pin definitions for the Z-80 microprocessor is provided in Table 4-1.

Both the Address and Data busses are buffered to enable them to drive the external chips of the system. The address bus, along with MREQ* and WR* are buffered by chips 1A, 2A and 3A. These chips are enabled by the inversion of BUSAK*. If the processor responds to a BUSRQ* signal, these chips will be turned off, or tri-stated. The data bus is buffered by a pair of bi-direct ional buffers. They are also turned off by the inversion of BUSAK*. The direction of the signal through the buffers is controlled by the WR* signal. Gating is provided to generate the signals IORD* (read From Input Port) and IOWR* (Write to Output Port). Gates are also used to buffer IORQ* and RFSH*. A crystal controlled oscillator composed of three inverters generates the CPU clock.

TABLE 4-1, PIN FUNCTIONS FOR Z-80 MICROPROCESSOR

PIN	MEANING
A0 - A15	Address Bus; this is a sixteen pin bus that is used by the Z-80 to address or select a specified device-RAM, ROM or I/O.
D0 - D7	Data Bus; This is an eight pin bus that is used to convey information between the Z-80 and other devices. It is bidirectional, meaning that data flows both to and away from the Z-80.
CLOCK (Φ)	This is a 2 MHZ signal which is used by the processor to time internal events. Everything occurs in multiples of the basic clock cycle. The amount of time required to execute a given instruction depends on the instruction type. Times from 3 to 21 clock cycles can be expected.
HALT*	An Output; This pin will go low when a Halt instruction is executed by the processor. All functions stop. The only way to get out of a Halt is to Reset, to interrupt, or use the non-maskable interrupt.
M1*	Machine Cycle One; This output signifies that the processor is doing an OPCODE Fetch, as opposed to a data read or write.
WAIT*	Upon receiving a WAIT* signal, the processor holds the data, address and control lines in the previous state for an extra clock cycle. If WAIT* is again true on the next clock cycle, the CPU again goes into a hold condition. If the WAIT* line is false, the CPU completes its instruction. This feature is used to hold the CPU if it attempts to access the video RAM during a video cycle.
BUSRQ*	This signal input (Bus Request) is used to signify that an external processor is going to take command of the bus. The Z-80 responds by completing the instruction in process, turning off its data, address, and control busses and bringing its BUSAK* (Bus Acknowledge) signal true. This condition is held until BUSRQ* is brought false. This feature is not used in the Astro-Invaders game.
NMI*	Non-Maskable Interrupt is an input that causes the processor to interrupt its normal program flow to respond to some special condition. Non-Maskable means that the processor cannot ignore it. Astro-Invaders does not utilize this feature.

TABLE 4-1, PIN FUNCTIONS FOR Z-80 MICROPROCESSOR (CONT'D)

PIN	MEANING
RESET*	This input is used to put the CPU into a known condition after power-up. Upon RESET* going false, the Z-80 will begin fetching instructions from address 0000H, in hexdecimal (base 16).
INT*	This input (Interrupt Request) signifies that something important is occuring. Upon receiving it, the CPU alters its instruction execution to service the interrupt. Interrupts occur at the middle of, and at the end of, the video screen. It should be noted that the interrupt is maskable, and can be ignored under software control. When the processor responds to an interrupt, it brings both its IORQ* and M1* lines true simultaneously.
BUSAK*	The Bus Acknowledge (output) is brought true in response to a BUSRQ* true signal.
RFSH*	This output signal (refresh) is brought true occasionally to assist in the refreshing of dynamic memories. When it occurs, MREQ* is also brought true. It is used only to insure that a CPU RAM cycle is a valid one, and not a refresh cycle.
MREQ*	The memory request output signifies that a memory access is being made.
IORQ*	The output (Input/Output Request) signifies that a peripheral access is being made.
WR*	The output (Write) is true whenever the CPU writes data.
RD*	The output (Read) is true whenever the CPU reads data.

* An asterisk is used in place of a bar (the NOT function) and indicates a signal which is true when at a logical zero.

Chip selects to the various PROM's and Scratch Pad RAM's are generated by a decoder. The inputs to the decoder are Address Bus bits A10, A11, A12, and A13, along with MREQ* and RFSH*. Only one of the outputs will be low at any one time, and only when MREQ* is true and RFSH* is false. These outputs enable the PROM's or RAM and gate internal data onto the bus (in the case of the PROM's and RAM read) or, in conjunction with WR*, write the data on the bus into the selected RAM location. +5 volts supplies all the chips while -5 and +12 volts are used only for the 2708 PROM's.

4.2 VIDEO BOARD

NOTE: The Video Board Schematic is presented at the end of this manual.

The video board is the most complex in the system and will be explained in the greatest detail. A video image is displayed on the CRT screen by sequentially reading out a group of Random Access Memory locations synchronously with the video beams, and then shifting the bytes out to the CRT a bit at a time. The resolution of the system is 256 dots or picture elements (pixels) per line, by 224 lines per frame. For every horizontal line displayed, the video RAM is read out 32 times.

The contents of the RAM is first latched into a shift register and then shifted out at the video rate of 4.915 MHZ, or 203 nanoseconds per bit. After the video "reads" have been completed, the hardware generates a blanking pulse to blank, or turn off the picture. Next, a horizontal synchronizing pulse is generated. This serves to return the beam of the CRT to the left hand side. The vertical counter is advanced, the blank pulse is ended, and the video RAM is again read out 32 times. Thus, a single horizontal line of video is generated. The complete process is repeated 224 times to display 224 lines of video. A vertical blanking pulse is now generated, followed by a vertical synchronization pulse. The vertical sync pulse returns the beam to the upper left hand corner to start another frame of video.

NOTE: The references herein to left hand and upper left corner of the screen refer to a monitor mounted in the normal manner or the same as that of a standard TV set. In Astro-Invaders, the monitor is rotated 90 degrees clockwise so the first horizontal line will start at the top right-hand of the screen and stop at the bottom right-hand.

4.2.1 Basic Video Cycle. The origin of all video timing signals is the 4.915 MHZ crystal controlled oscillator. The signal is generated by inverter 2E, and is fed to the horizontal address counter 2D, as well as the two video shift registers 1A and 2A. This signal is referred to as PIXCLK on the video board schematic and block diagrams. With reference to Figure 4-1, (Basic Video Clock Cycle Diagram) it should be noted that there are 8 PIXCLK cycles to each video cycle.

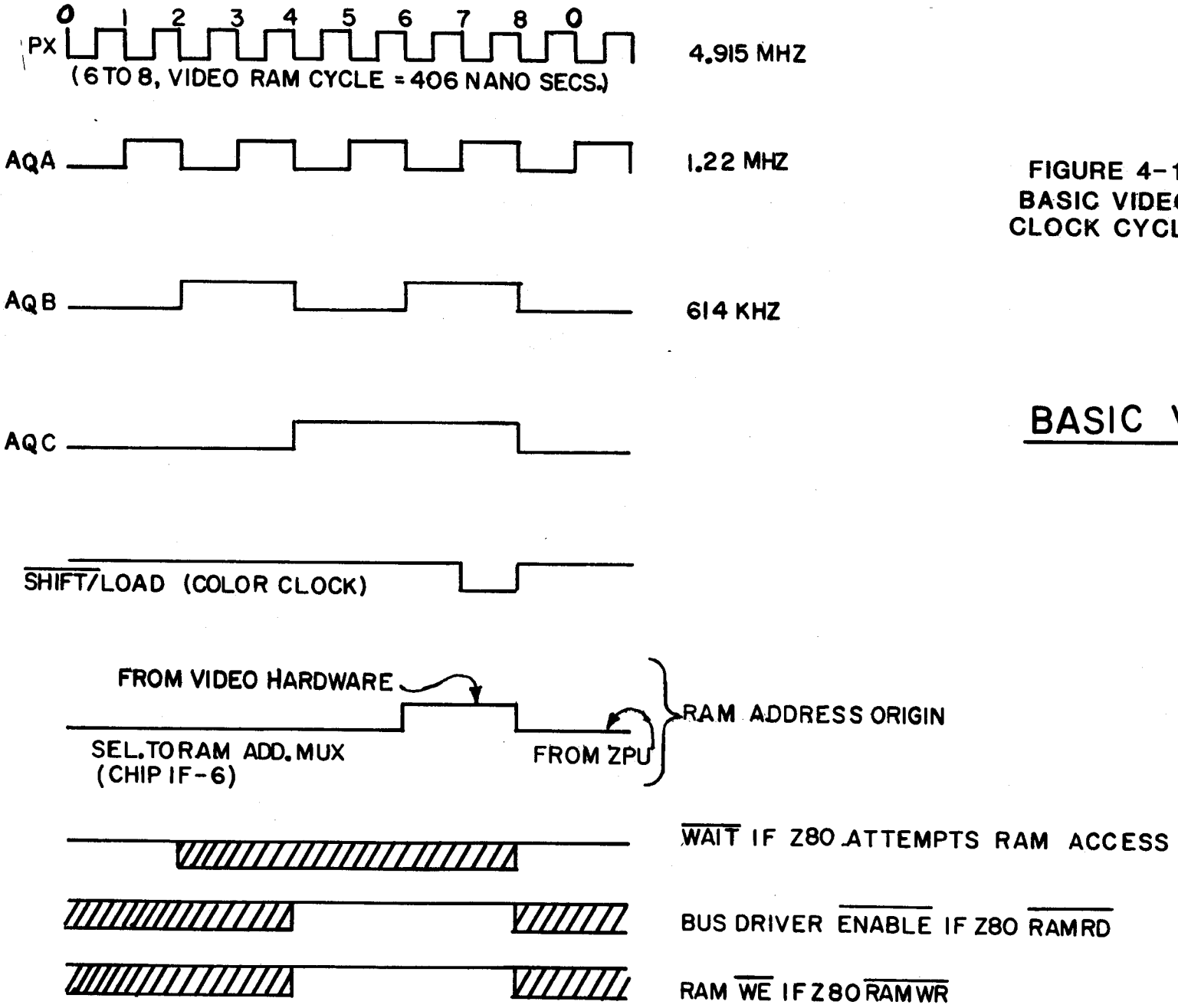


FIGURE 4-1
BASIC VIDEO
CLOCK CYCLE

BASIC VIDEO CYCLE

The outputs of Horizontal Address Counter 2D designated as AQA, AQB and AQC define the video cycle. At count 6, the actual RAM cycle occurs. AQB and AQC are gated together by AND gate 1F to generate a "one" going signal to the RAM Address Multiplexers 5A, 6A, 7A, and 8A. The select (S) input is this signal, and at the time it becomes a "one" it selects the address counters as the RAM addresses instead of the CPU bus. The CPU bus is selected when "S" is a zero. After the RAM data are stable, it is strobed into the Video Shift Registers at count 7 of the video cycle. This SHIFT/LOAD* signal is generated by NAND gate 1D.

If the Z-80 attempts to access RAM any time during PIXCLK counts 2 through 7, the CPU will be put into a WAIT* state by the RAM access arbitrator, made up of OR-gate 2C and NAND gate 1G. Address decoding circuitry comprised of inverter 2E, and NAND gates 1D and 1G signal the fact that the Z-80 is attempting a RAM access. The generated WAIT* state will end when state 0 occurs. On Figure 4-1, the WAIT* state and the three following waveforms are presented in shaded form since they can occur any time during the shaded area - the CPU is completely asynchronous to the video timing signals.

Once the Z-80 gains access to the RAM, it either reads or writes data. Gating comprised of inverter 3F, AND gate 1F, inverter 3F, and OR gate 2F combine the previously decoded CPU RAM SELECT Signal, video horizontal address counter output AQC, and CPU Control line WR* to generate CPU RAM WRITE*. This signal writes data present on the RAM Data Input lines (CPU Data Bus) into the locations addressed by the RAM Address Bus-which now originates from the CPU Address Bus-since the "S" or VIDCYC line of RAM Address Multiplexers 5A, 6A, 7A and 8A is at a zero (selecting the "A" inputs).

If the CPU is in a read operation, the address still originates from the CPU Address Bus but instead of writing Data Bus data, NAND gates 2G generate a CPU RAM READ* which causes the tri-state buffers to drive the RAM data (now on the RAM Data Output bus) to the CPU Data Bus. These tri-state drivers are gates 3A and 4A. Under all other conditions, Buffers 3A and 4A are disabled. This disabling permits the CPU to have full access to the data bus. It should be noted that the bottom two waveforms of Figure 4-1 cannot occur simultaneously since one occurs when WR* is true and the other when WR* is false.

4.2.2 Ram Horizontal Address & Sync Circuitry.

NOTE: In this and all following sections, references to Horizontal, Vertical, and to "areas of the CRT screen" are presented on the basis that the monitor is mounted in its normal or "TV-like" position. This position must be rotated 90 degrees clockwise for the actual displayed conditions.

As stated earlier, all RAM addresses originate at either the CPU Address Bus or the Horizontal and Vertical Counters. RAM Address Multiplexers 5A, 6A, 7A and 8A determine this origin under the control of the VIDCYC signal as explained earlier. The Video Address Bus is selectively inverted by exclusive - OR gates 5D, 6D, 7D, and 8D and by the Full-Adder 7E. These circuits will be explained later (Refer to the UPRIGHT*/FLIP logic in paragraph 4.2.4).

Horizontal Addresses originate in counter 2D, bits AQD, BQA, BQB, BQC, and BQD, which become Video Address bits AB0, AB1, AB2, AB3 and AB4, respectively. These address bits have 32 possible values from 00H to 1FH. AB0 is the least

significant bit while AB4 is the most significant. With reference to Figure 4-2, the numbers above the AB0 waveform are the actual hexadecimal addresses generated by the various combinations of AB0 through AB4. Note that VIDCYC signals are being continuously generated, resulting in video RAM read cycles, but only the addresses shown in Figure 4-2 are actually displayed. Also, note that address 00H is displayed twice. Relating this to the TV screen, address 00H will be displayed in the left hand (convert to right hand per note) edge and address 1FH is displayed in the right hand edge (convert to bottom). Anytime the signal HBLANK* latch is false, video is displayed. When HBLANK* latch is true, the CRT is blanked.

In Figure 4-2, a sharp spike can be seen on the AB3 waveform. This is actually a propragation delay spike, since AB3's zero-to-one transition results in the clearing of the Horizontal Address counter which returns AB3 to a zero. Specifically, AB3 is inverted by inverter 4F, resetting RS latch 5F. This causes the zero-to-one transition of HBLANK* latch, which unblanks the video. Also, a differentiated pulse is received from an R-C network which is connected to the latch and clears the Horizontal Counter, via inverter 4F. The Horizontal counter now increments through addresses 00H to 1FH. AB4's one-to-zero transition at the end of state 1FH causes J-K flip-flop 6E to transition, resulting in a "one" on its Q output. This signal is gated with AB0 in NAND gate 5F, which sets HBLANK* latch 5F when AB0 goes to a "one". This results in Video blanking. Nothing further occurs until AB0 again returns to a "one".

Inverter 2E, along with AND gate 1F combine AB1 and AB2 such that its output is at a "one" during the time the Q output of flip-flip 6E is at a "one". These two signals, along with AB0 are combined in NAND gate 1D. Finally, when AB0 returns to a "one", NAND gate 1D's output goes to a zero. This causes three things to happen: (1) HSYNC* is generated, (2) the Vertical Address counter is advanced and (3) J-K flip-flop 6E is cleared. HSYNC* is combined with VSYNC* in NAND gate 2G, and inverters 5A, 8G, and 6G to form CRT HVSYNC* to the monitor. HBLANK* is combined with VBLANK* in NAND gate 1G. This is inverted by 4F to form COMPBLANK* which holds the Video Shift Registers cleared during blanking and synchronizing of the monitor.

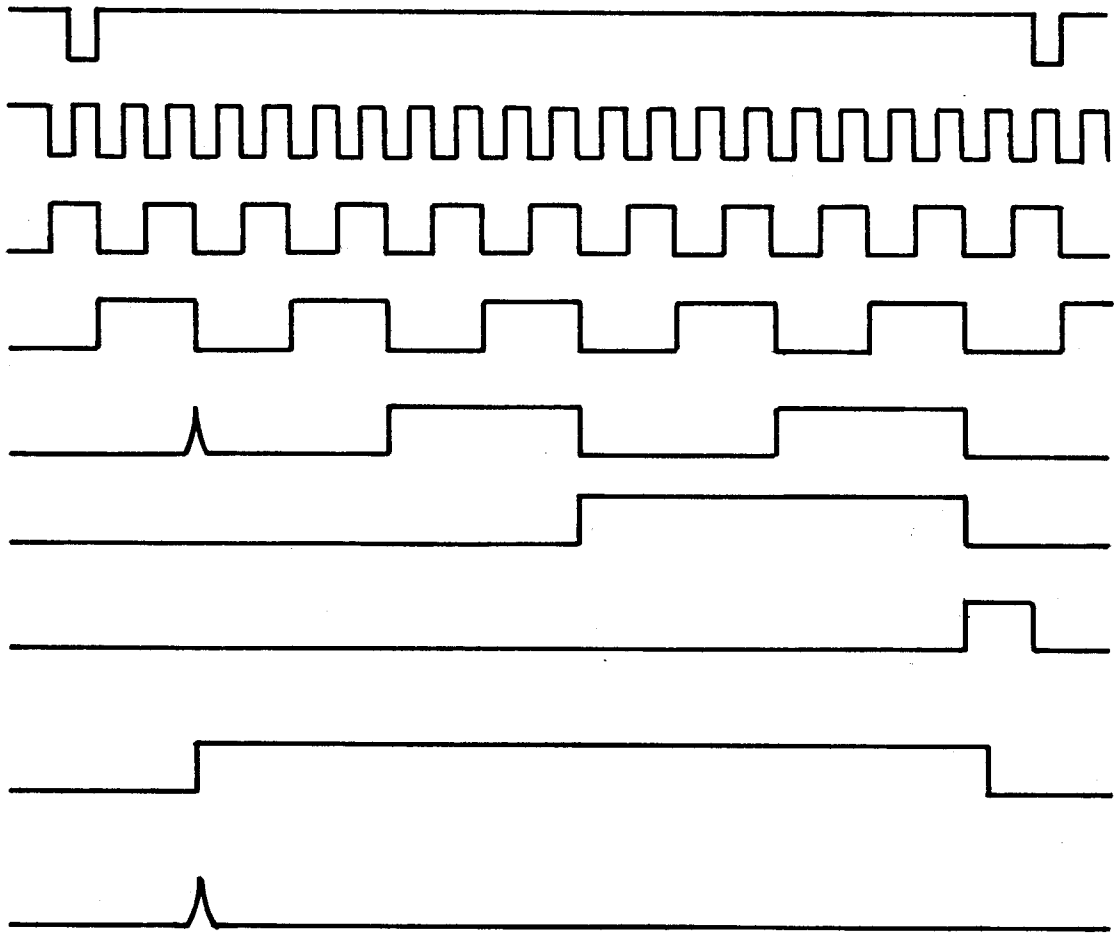


FIGURE 4-2
HORIZONTAL COUNTER
CIRCUIT TIMING

TIMING DIAGRAM
HORIZONTAL CIRCUITRY

ASTRO-INVADERS 6-21-80

4.2.3 Ram Vertical Address. As previously stated, the Vertical Address Counter (4D) is clocked by HSYNC*. Thus, for every horizontal line of 32 RAM Accesses, the counter is advanced for another 32 RAM Addresses. The displayed portion of the Vertical Address Counter range is 224 lines. However, the counter actually counts through 256 states. Inverter 3F is connected to the clear pins of the Vertical Address Counter but it does nothing. Video Address bus bits AB5 through AB12 are generated by this counter. Only waveforms AB8 through AB12 are shown in Figure 4-3 for clarity. Video is only displayed when VBLANK* latch is false. The VBLANK latch 3D is set by AB12's one-to-zero transition, through an R-C differentiator. Again, this brings VBLANK* true, which causes blanking by clearing the Video Shift Registers. Address bits AB8 and AB9 are combined by inverter 2E and OR-gate 2C which results in a zero-going signal whenever AB8 is a "one" and AB9 is a zero. This signal is gated with the inversion of VBLANK* (itself the inversion of VBLANK) in OR-gate 2F, resulting in VSYNC*. VSYNC* is combined with HSYNC* as explained earlier to form the composite sync to the monitor.

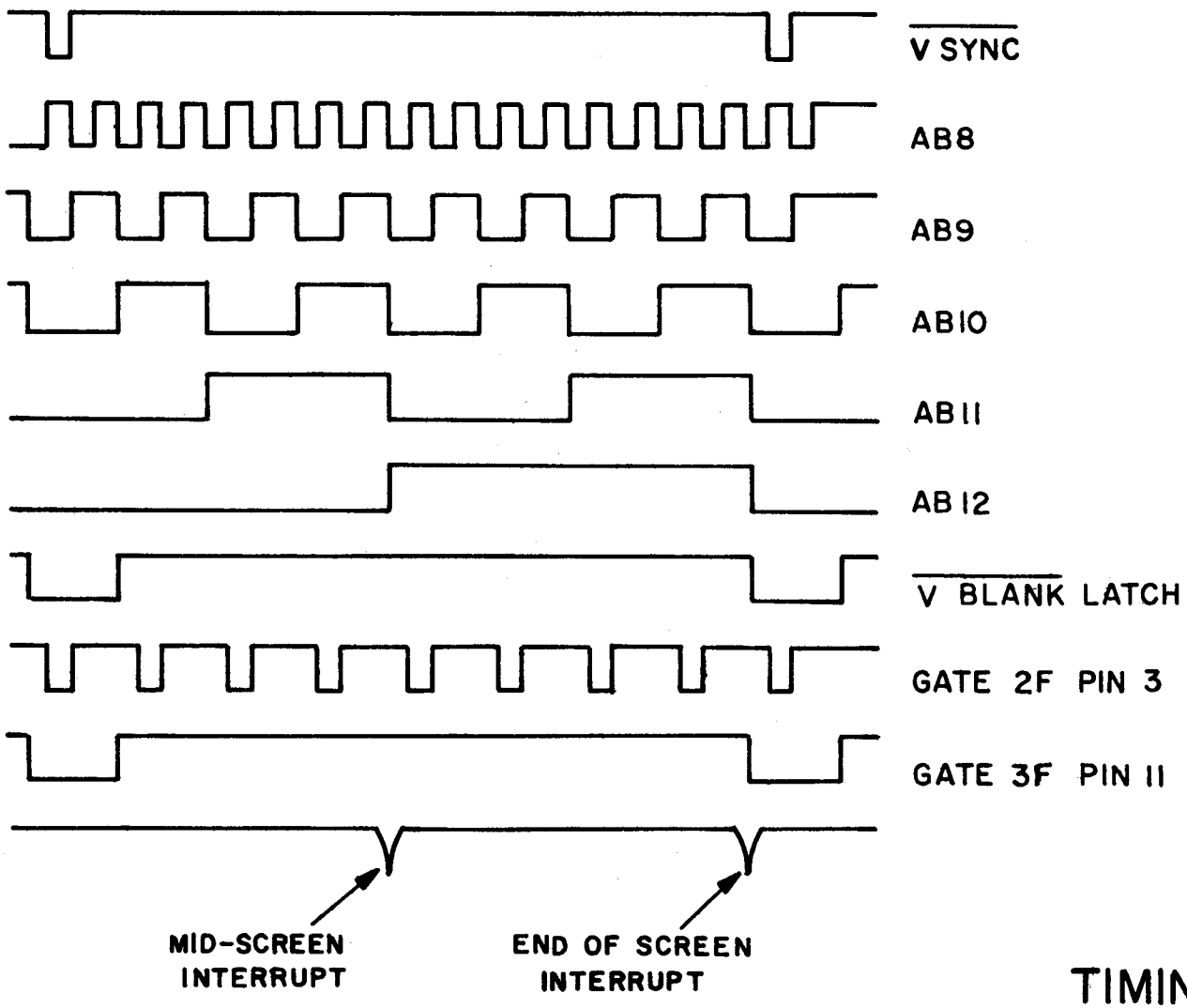
VBLANK* becomes false when AB10 goes to a "one" following VSYNC*. This is accomplished by AB10's inversion through 3D, resetting VBLANK* latch 3D. Note, however, that AB10 is a "one" at the start of displayed video. This relates to the actual starting address of the Video RAM within the Video Address Counter, and hence in the CPU Address Bus. The actual starting address of the Video RAM is 400H for the Video Address Counter, and 2400H for the CPU Address Bus. Thus, the upper left hand portion of the screen corresponds to address 2400H (400H to the Video Address Bus) and the upper right hand portion is 241FH (41FH). The lower left hand corner is 3FE0H (FE0H) and the lower right hand corner is 3FFFH (FFFH). Bit 0 of each of these addresses is the left hand most bit, while Bit 7 is to the right. NOTE: The foregoing description is for either an upright game or a cocktail game while acting as player number one. Displayed addresses will change when acting as player number 2 on a cocktail table version of the game (See the section on Flip Logic for more details).

Since AB12 is the chip select to both sections of the video RAM, the video displayed in the upper half of the screen is stored in RAM's 1B through 8B, while video displayed in the lower half of the screen is stored in RAM's 1C through 7C. The contents of individual RAMS actually form vertical bands on the screen, repeating every eighth pixel.

The paragraph on Interrupts, in the CPU Board Theory-of-Operation, discussed a midscreen and end-of-screen "interrupt". These interrupts are used for general timing applications by the software and are generated by OR-gate 8E, XOR gates 8D, and an R-C integrating network: OR gate 8E acts as a buffer while XOR gate 8D is a frequency doubler and pulse stretcher. The latter circuit outputs a "one-going" pulse whenever AB12 goes through a transition. XOR gate 8D (pins 1, 2 & 3) acts as an inverter, the output of which is the actual interrupt to the CPU. Its waveform is shown at the bottom of Figure 4-3.

4.2.4 Flip Logic. When the Astro-Invaders game is packaged in a cocktail table, a flip of the video occurs whenever the active player changes sides. This presents the proper game display for players sitting on opposite sides of the table. The UPRIGHT Cabinet game does not require this feature and the circuit is strapped low.

FIGURE 4-3
VERTICAL CIRCUIT TIMING



VERTICAL
RESOLUTION= 224 LINES

TIMING DIAGRAM
VERTICAL CIRCUITRY

ASTRO-INVADERS 6-21-80.

An output bit on the I/O Sound Board is defined as the UPRIGHT*/FLIP bit and it implements a hardware inverstion of the video picture. This is accomplished by inverting or complementing the entire Video Address Bus. The net effect is to cause the counters to decrement from a maximum value, instead of incrementing from a minimum value. In other words, as far as the RAM is concerned, the counters are running backwards. The upper left hand corner of the screen is now FFFH, the upper right hand corner is FE0H, the lower left hand corner is 41FH and the lower right hand corner is 400H.

The hardware implementation of the flip is to connect all bits of the Video Address Bus to XOR gates 5D, 6D, 7D and 8D and to connect the outputs to the RAM Address Multiplexers. If the control input to the XOR's is a zero, the addresses are fed through unaffected. If the control input (the UPRIGHT/FLIP*) is a one, the addresses are inverted. Full Adder 7E compensates for the fact that the screen starts out at an address of 400H. (Since Address bit AB10 starts at a 1 for the beginning of the screen, it will become a zero through XOR gate 7D. Adder 7E adds a constant 1 (equivalent to 400H) to the top 3 bits of the Address bus to compensate, resulting in FFFH for the top left corner.

To implement a flipped image it is not adequate to merely complement the Ram Addresses. The resulting RAM data must also be shifted in reverse order. In addition, the color look up information must be flipped. This function is performed by two VideoShift Registers, one shifting from bit 0 through bit 7 (normal video) and the other shifting from bit 7 through bit 0 for flipped video. The color look up PROM is set up so the color data on the upper 3 output bits (for normal video) are reflected (or flipped) for the flipped video action. Multiplexer 5E selects the Video Shift Register as well as the set of color look up bits required for each condition.

4.2.5 Color Output. The serial Video stream generated by the selected Video Shift Register is gated with the output of the Color look up PROM (Chip 3E) to generate one of eight colors on the screen. The screen is divided into 896 color blocks with each block 8 pixels wide by 8 high. A pixel bit having a value of one (in any block) will be gated through to the monitor with the R, G, and B values given by the look-up PROM. A pixel of zero value will produce a black spot.

The addresses for Color look-up PROM 3E come from Video Address bus bits AB0 through AB4, which provide 32 horizontal areas. Bits AB8 through AB12 provide 32 (actually 28 due to the starting state of AB10 as described previously) vertical areas. For each area, a color bit value is selected with the value 0 (Black) through 7 (white). The D type flip-flops (6F and 7F) latch the color value every time the Video Shift Registers are loaded. Their outputs are then combined with the "RED SCREEN" signal.

During the game a "RED SCREEN" occurs whenever an enemy invader, or part of an invader's explosion, hits the player's base or tank. A "RED SCREEN" will also occur if the UFO reaches the bottom of the screen. This, along with an explosion sound, signifies the loss of a base. An output port on the I/O Sound Board results in the "RED SCREEN" signal. OR gate 7G will output a logic one under this condition (whether or not the actual color has red set). NAND gates

8F force the Green and Blue off. The outputs of the latter gates are combined with the inversion of serial video (provided by 8G) via OR gates 7G. If a color is to be displayed, the output of the OR gate will be zero. These signals are inverted by open-collector inverters 6G, and applied to the monitor at the 10-pin KK100 connector.

4.2.6 Miscellaneous Circuits. Power for the board is received through the Mother Board bus. The +5 Vdc power is used by all the circuits while -5 Vdc and +12 Vdc are required only by the color look up PROM. Although one output of the HBLANK* latch is connected to the BUSREQ* pin on the mother board, this feature is not operational since it is disconnected at the CPU Board.

4.3 I/O SOUND BOARD

The I/O Sound Board contains all the Input/Output interfaces of the system as well as all the sound generating circuitry. Refer to the schematic diagram at the end of this manual.

The actual interface to the processor is accomplished by the use of two 8255 Peripheral Interface Adapter's (PIA). As configured in Astro- Invaders, each PIA is used as either an input or output port but the PIA can actually be used as a bi-directional port with proper control signals.

All eight bits of the data bus connect to each PIA, as does A0, A1, IORD*, IOWR*, AND RESET. As explained in the CPU Board Theory-of-Operation paragraphs (4.1), Input/output ports are handled differently as compared to memory. When the CPU board attemps to read an I/O port, it will bring IORD* true. Conversly, when an I/O write occurs, IOWR* is brought true. RESET initializes the PIA to a known state. Address bus bits A0 and A1 select registers internal to the PIA. Address bit A2 is used as a chip select (along with either IORD* or IOWR*) to the input PIA. Address bit A3 is the corresponding chip select to the output PIA. Processor addresses for the I/O ports are as follows:

INPUT PORT A :	08H
INPUT PORT B :	09H
OUTPUT PORT A :	04H
OUTPUT PORT B :	05H

4.3.1 Input Ports. PIA "A" (chip #20 on the I/O Sound Board) is the input Port. It receives information from the player switches, coin switch, etc. Inputs from all player controls are handled in like manner and, therefore, only one of eight identical circuits will be explained. All player controls provide switch closures to ground. When closure occurs, a 3.3 microfarad capacitor is discharged through a 100 Ohm Resistor in series with the switch. When the voltage level on the capacitor drops below the low going threshold of the 74LS14, (approximately one volt) the 74LS14 output will switch to a logical one. The CPU constantly monitors the input ports (as a result of its interrupt routine) and will respond according to which switch is closed. When the switch opens, the capacitor is recharged through the 100 ohm and a 1000 ohm resistor to the +5 volt supply. When the charge across the capacitor reaches the high going threshold of 74LS14, (approximately two volts) its output will switch to a logical zero.

The processor is now aware of the fact that the switch is open, and ceases its response. The game setting switches simply apply either a logical one or zero to the input port bit. A pull-up resistor is provided to insure a logical one when the switch is open.

The coin switch operates in a similar manner and uses a similar R-C debounce circuit. The output of the debounce circuit is connected to a driver transistor used to advance the coin counter. This output is available on pin 8 of the Input/Output connector. An anti-kickback diode is also mounted on the board. It's anode is connected to the counter output transistor collector. The cathode is connected to pin 6 of the same connector. The debounce circuit output is also connected to the clear input of a 74LS123 one-shot. This one-shot is used as a pulse stretcher to insure that the processor is made aware of a coin drop. When the debounce circuit output goes to a logical one, (as explained above), the clear signal is removed from the one-shot, causing it to start a timing cycle. This timing cycle will last for approximately 28 milliseconds during which time the Q output will be a logical zero. This output is combined with the service switch input at NAND gate 18 and the result is applied to port A, bit 0, of the input port. The service switch will add credit but will not advance the coin counter.

4.3.2 Output Ports. All bits of each output port are used for sound generation except for port 8, bit 5, which is used as the UPRIGHT*/FLIP control bit. Its output is inverted, then applied to the game cabinet jumper select. If the connection between the inverter and the edge connector (Pin 41) is broken, and the edge connector grounded, the game is set up as an upright, and the picture will not flip between players. Conversely, if the connection is not broken, the picture will flip between players.

Port A, output bit 2 controls the missile explosion sound. It is also connected to the bus connector (pin 23), and becomes the RED SCREEN control bit. When this sound effect is generated, the screen turns red. See paragraph 4.2.5 for details.

4.3.3 Fire And Tank Explosion Sound Generation. The"Fire" and "Tank Explosion" sounds are generated in a similar manner since they both use a noise generator consisting of an oscillator made up of two 74C86 XOR gates (chip #4) which clock a CMOS 4006 Shift Register. Two outputs of the shift register, Q17 and Q19, are combined in an XOR gate and fed back to the input, D5. The shift register and XOR feedback make up a psuedo-random noise generator. A network made up of a 0.1uF capacitor, two diodes and two resistors (1 MEG and 270K ohm) insure that the shift register does not come up in an illegal state (e.g., all Q's at zero). One of the shift register taps (Q13) is used as the output of the noise generator and is input to both the Fire sound generator and the Tank Explosion sound generator.

The control circuitry for the Fire sound generator, the Tank explosion sound generator and the "Invader Destroyed" sound use similar circuits. Any one of these circuits operates as follows: The output bit of PIA B connects to an open-collector buffer (type 7407). Normally, the buffer output is on, which disables the sound generation. When the PIA Output Bit is written to a one, the buffer turns off, enabling the sound. A 1K ohm pull-up resistor at the buffer

output provides a one-going signal which is differentiated by the following R-C network. This provides a positive going pulse to the non-inverting input of an OP-Amp (chip 9 for both generators). The OP-Amp output now goes positive, which is fed back by a 1 megohm resistor to the non-inverting input. This "Hysteresis" action has a latching effect, holding the output high. The high going output also charges a timing capacitor connected to the Op-Amp's inverting input through a 560K ohm feedback resistor. The capacitor value and the associated bias network determine the time constant of the circuit. When the capacitor charges to the voltage on the non-inverting input of the Op-Amp, its output returns low, discharging the capacitor. This circuit is then a triggered one-shot, whose time constant is determined by the capacitor and biasing network.

In the case of the Tank Explosion Sound, the output of the one-shot is put through a diode, resistor and capacitor and applied to pin 10 of Op- Amp 9. The output of this network (as applied to pin 10) will go to a logic one at the time of the one-shot output, and will decay off to a zero when the one-shot output goes back to zero. This envelope is applied to Op-Amp 9, which sums it together with the output of the noise generator. The Op-Amp output is a low-pass, filtered signal which is applied to Sound Adjust Potentiometer VR1.

The output of the "Fire" sound one-shot (also chip 9) is applied to a short-time envelope generator made up of Norton-Amp 10. Its output is much the same as the diode, capacitor and resistor network mentioned earlier, but has a shorter time duration. Other Norton amplifiers in chip 10 wave shape and amplify the output of the noise generator. This output together with the decaying Norton Amp output envelope is applied to a summing amplifier (Norton Amp 10, Pins 2, 3 and 4). This decaying, filtered noise envelope is applied to Op-Amp 9 at pin 6 together with another decaying envelope (originating at the Fire sound 7407 buffer and applied through a diode, capacitor and resistor network to pin 5). The signals at pins 5 and 6 are summed together and the output (pin 7) is a high-pass, filtered signal that is applied to Sound Adjust Potentiometer VR2.

4.3.4 Invader-Destroyed And UFO Sound Generation. The basis of the invader-destroyed and UFO sounds is a Voltage Controlled Oscillator, or Sweep oscillator, made up of Op-Amp 6 (pins 1, 2 and 3) and Norton-Amp 5. The Op-Amp generates triggers to initiate a sawtooth waveform generated by the Norton-Amp (pins 10, 11 and 12). This sawtooth is then applied to pins 1, 6 and 5 of chip 5. This stage, along with the stage using pins 2, 3 and 4, plus a transistor, forms the actual oscillator circuit. The frequency of oscillation is determined by the sawtooth waveform voltage and the transistor. When the output voltage at chip 5, pin 5, reaches a value determined by the biasing of chip 5 pins 2, 3 and 4, the transistor is turned on which results in a negative going ramp at pin 5. When the sawtooth voltage is reached, the transistor turns off, and the ramp starts to go positive again. The output at pin 5 of chip 5, is applied to the "Invader Destroyed" and "UFO" sound generators.

The Invader Destroyed Control circuit (through a 7407 buffer, pins 12 and 13) is the same type of triggered one-shot as explained previously for the Fire sound except that the time constant has been altered. The output is connected to a triangle generator (chip 5 pins 8, 9 and 13), the output envelope of which

is summed together with the VCO output by chip 6 pins 5, 6 and 7. The output signal is a high-pass filtered version applied to potentiometer VR4. The UFO sound is normally disabled by a conducting transistor which shorts the sound to ground. Isolation between this circuit and the voltage controlled oscillator (VCO) is provided by a 22K ohm resistor. When the processor writes output port A bit 0 to a one, the inversion provided by the 74LS14 (chip 14) turns the transistor off. The VCO output can now pass through the high-pass filter and be applied to sound adjusting potentiometer VR5.

4.3.5 UFO-Destroyed Sound. The control circuit for this sound uses a 7407 open-collector buffer (pins 5 and 6) to start and stop a triangle generator (chip 7 pins 8, 9 and 13). The output of this triangle generator is applied to Summer chip 8 pins 1, 2 and 3. Another VCO is made up of chip 7 (pins 2, 3, 4; 1, 5, 6; 10, 11, 12), chip 8 (pins 12, 13 and 14) and a transistor. This VCO operates in like manner to the UFO sound generator, except that the time constants are charged to vary the frequency and sweep rate. The UFO-destroyed VCO output is also applied to the Summer circuit (chip 8 pin 2). The Summer output is high- pass filtered, and applied to Sound Adjusting Potentiometer VR3.

4.3.6 Invaders-Advancing And Bonus Sound. The "Invaders-Advancing" sound is generated by one half of a 556 (chip 11) dual timer. The timer is set up as a standard astable multivibrator, except that the charge time constant is variable as controlled by PIA B. The discharge time constant is fixed by the 75K ohm resistor between pins 12 and 13 of the chip. PIA output Port-B, Bits 0 through 3 control the charge time by switching in various resistor values to the +5 volt supply. Four open-collector buffers (7407, chip 15) isolate the pulled-up resistors from the PIA, while diodes isolate the pulled-down (or switched out) resistors from the 556. Sixteen possible charge rates are provided by enabling various combinations of the four circuits. The output of the 556 is buffered by gate 3 (a 7411), band-pass filtered and applied to setting pot VR6.

The Bonus sound is generated by the other section of the 556 dual timer in conjunction with a 555 timer. Both timers are configured as astable multivibrators, but with different repetition rates. PIA Port B bit 4 enables this section of the 556 by removing the logical zero from reset pin 4. The 555 (chip 13) free-runs. The enable line (Port B bit 4), the 556 output and the 555 output are combined in AND gate 13. The output is buffered by another AND gate (chip 13), high pass filtered, and applied to sound setting potentiometer VR7. AND gate 3 (pin 12) will be a a logic one only when both oscillator outputs and the enable are at logic ones.

4.3.7 Audio Summer And Power Amplifier. The slider of each VR potentiometer (mentioned in previous descriptions) is connected to a common point through 22K ohm resistors and a 1 microfarad capacitor. This common point is the inverting input of Op-Amp 2 (pins 1, 2 and 3). Potentiometer VR8, in the feedback circuit of the Op-Amp, sets the master volume. The output of this amplifier feeds one input of a Power Amplifier (chip 1 pin 7). An inverting Op-Amp (chip 2 pins 12, 13 and 14) feeds the signal to the other Power Amplifier input.

A sound enable control is implemented by chip 15 (a 7407), a pull-up resistor, and two diodes which connect to the inverting inputs of both Op-Amps. Any time the buffer chip produces a logic zero at its output, the inverting

Op-Amps and hence the Power Amplifier are enabled. When the 7407 is off, the pull-up resistor and diodes swamp the Op-Amp inputs, taking their outputs low. The open-collector buffer is controlled by a NAND gate (chip 18). One of its inputs is connected to an R-C network that forces the NAND gate output high for a period of time when power is first applied to the game. This mutes, or turns off the Power Amplifier. After the capacitor has charged, the processor may enable or disable sounds by writing bit 5 of output Port A to a logic one or a zero, respectively. Each output of the Power Amplifier is connected to one terminal of the speaker to form a bridge configuration. The inverting stage provided by Op-Amp 2 (pins 1, 2, 7, 3 and 14) forces the amplifier outputs to be out of phase by 180 degrees, causing one side of the speaker to be driven high, while the other side is driven low.

4.3.8 Power Requirements. The two 8255 PIA's, the 7407's, the 555, 556, 74LS14's, 74123, 7411 and 74LS00 are supplied by the +5 volt regulated supply as distributed via the Mother Board interconnection busses: All other circuitry, with the exception of the Power Amplifier itself, is driven from the +12 Volt regulated supply as distributed via the Mother Board interconnecting busses. The Power Amplifier receives power from the VAUDIO (+15 max.) supply, brought in through the I/O Sound Board edge connector.

4.4 POWER SUPPLY

4.4.1 Operation On 120 Or 240 Vac. The power transformer has a split primary winding which must be connected in parallel for a 120 Vac line or connected in series for 240 Vac operation. A 6.3 Vac secondary (10 & 11) provides power for general illumination on the coin door. A 120 Vac secondary (12 & 13) is used as an isolation winding for powering the monitor.

4.4.2 5 Volt Supply. An 8 Vac winding is used as the logic power supply and is protected by F3, a 5 amp fuse. A full wave bridge rectifier (diodes CR1 through CR4) rectifies this voltage and capacitor C1 filters it. This voltage is +5 unregulated and is available at pin 1 of J3 and J4. This voltage is also connected to the +5 volt regulator which is mounted on a separate heat sink. A 5 volt adjustment pot (R2) is provided to insure that the supply voltage is proper at the load. The supply is adjusted so that +5 volts is actually applied to the game logic boards. This usually means that the voltage measured at TP1 of the power supply is +5.3 to +5.5 VDC. The +5 volt regulated supply is available at jacks J3, J4 (pins 2, 3 and 4).

4.4.3 Positive 12 Volt Supply. A center - tapped secondary of the transformer (terminals 7, 8 and 9) supply the other voltages required for the game. The center tap is grounded. Diodes CR5 & CR6 make up a positive full-wave rectifier. Fuse F1, a 3 Amp Slo-Blo, protects the positive supply. Capacitor C2 filters the +12 unregulated supply, which is available at jacks J3 & J4 (pins 14). This supply is connected to two regulators, VR1 & VR2, which are mounted on a heat sink on the Power Supply P.C. Board (PS-1000). VR1 is a +12 volt regulator, with output available at jacks J3 Y J4 (pins 6 & 7) and a voltage test point for measurement at TP4. The voltage measured should be between +11.4 and +12.6 volts Vdc. VR2 is a +15 volt regulator which receives its power from a +12 Vdc unregulated supply. Its output is measured at TP3. This regulator is used to limit the maximum voltage available to the Power Amplifier to protect it. The regulator output is generally +8 Vdc to +14 Vdc.

4.4.4 Negative 12 Volt and 5 Volt Supplies. Diodes CR7 and CR8 form a negative, full-wave rectifier, protected by fuse F2, a 3/4 Amp Sl-Blo type, and filtered by C3. This -12 volt unregulated power is available at J3 & J4 (pin 15). Voltage regulator VR3, a -5 volt regulator is fed by this supply and its output is available at jacks J3 & J4 (pins 5 and 8). This voltage can be measured at TP2, and should be between -4.75 and -5.25 Vdc. All four of the voltage regulators contain over current shut-down circuits.

Care should be exercised when working in the area of the power transformer since line voltage is available at terminals 1, 2, 3, 4, 12 and 13 of the transformer. It should also be noted that lethal voltages are available at several places on the color monitor.

SECTION 5
MONITOR ADJUSTMENTS

5.1 GENERAL INFORMATION

The display monitor used in this game is a 19" Wells-Gardner in-line color video unit with separate Red, Green, Blue and composite Sync inputs. Input signals on these lines must be at TTL levels.

5.2 POWER REQUIREMENTS

The monitor requires 120 Vac 50/60 Hertz for operation. Maximum power consumption is 103 watts. The power transformer has an extra winding to isolate the "hot" chassis of the display monitor from the power line and logic ground. The split primary of the power transformer provides a means of adjustment for operation on 220 Vac 50/60 Hz.

5.3 DEGAUSSING

The display monitor is equipped with a degaussing coil that automatically demagnetizes the picture tube during power up when the game has been de-energized for more than five minutes. However, an occasional manual degaussing is required to compensate for stray magnetic fields and disturbances. The procedure utilizes a user provided manual degaussing coil which is slowly moved in a circular motion around the various surfaces of the monitor. Use care to avoid contact with any high voltage points. The procedure is concluded by moving the coil away from the monitor to a minimum distance of six feet and then removing the power.

5.4 PURITY

If degaussing the monitor fails to improve bad color, a purity adjustment may be required. To perform this adjustment, first position the game so the monitor faces either north or south, then use the following steps.

1. Remove the cable assembly from the monitor input connector.
2. Turn the red Cut-Off Control (VR403) on the neck board fully CCW. Turn the green and blue Cut-Off Controls (VR404 & VR405) fully clockwise.
3. Pull the yoke backward until a magenta belt appears on the screen.
4. Adjust the purity rings until a red area is centered on the screen.
5. Push the yoke forward until the red area just fills the screen, then tighten the yoke.

5.5 CONVERGENCE

To insure that the three electron beams are correctly aligned at all parts of the screen, a convergence adjustment should be made. Proceed as follows:

1. Connect a cross-hatch signal generator to the monitor.

2. A pair of 4-pole convergence magnets are provided and should be adjusted to converge the red and blue beams. When the Pole is opened to the left and right (45 degrees symmetrically), the magnetic field is maximum. The red and blue beams will be moved to the left and right oppositely (See Figure 5-1). Adjusting the angle between the tabs will adjust the convergence of the red and blue vertical lines. When both the 4-pole convergence magnet tabs are rotated as a pair, convergence of the red and blue horizontal lines will be adjusted.

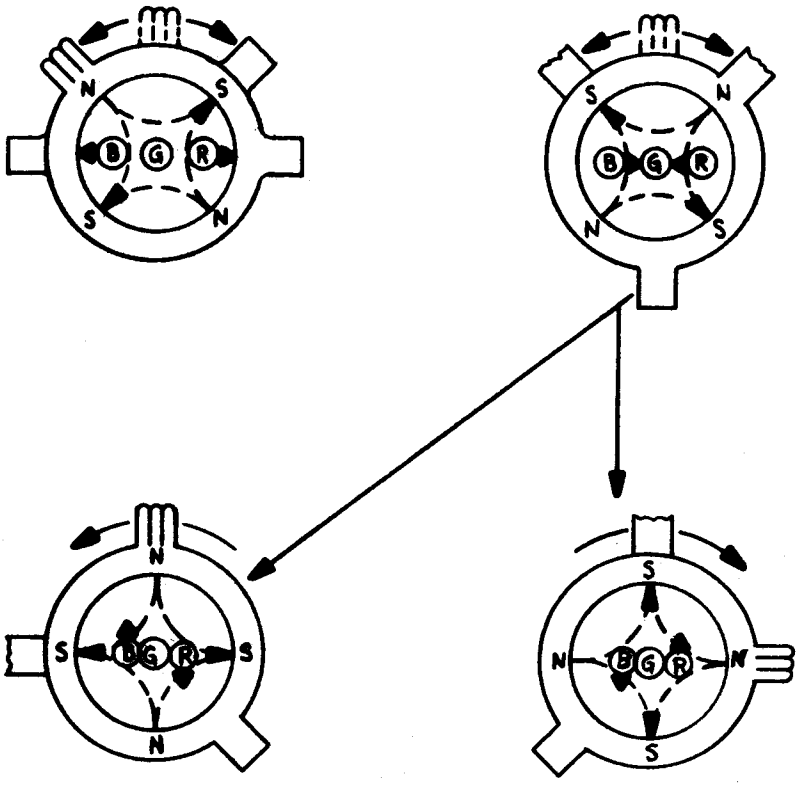


Figure 5-1, 4-Pole Convergence Magnets

3. A pair of 6-pole convergence magnets controls convergence of the magenta (red and blue) to green beams. When the pole is open to the left and right 30 degrees, symmetrically, the magentic field is maximum. The red and blue beams move to the left and right (See Figure 5-2).

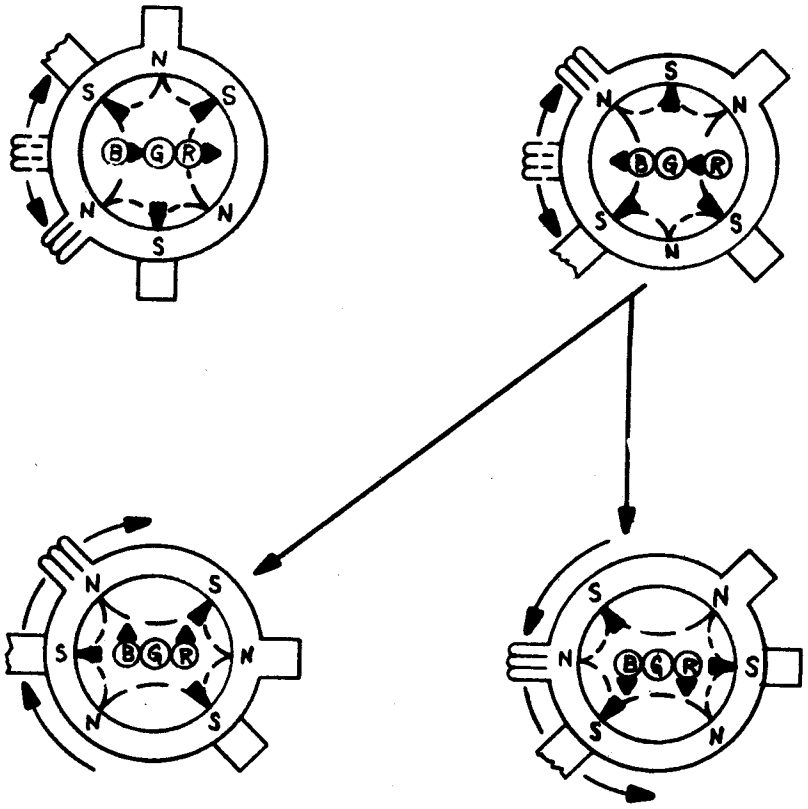


Figure 5-2, 6-Pole Convergence Magnets

Adjustment of the opening angle will adjust the convergence of the magenta to green vertical lines. Rotating both 6-pole convergence magnet tabs as a pair will adjust the convergence of the magenta to green horizontal lines.

5.6 BLACK AND WHITE TRACKING

Adjust the color balance of the display monitor as follows:

1. Ground the R, G, and B inputs.
2. Set the Black Level Control (VR201) to its mid point.
3. Set the Red and Blue Drive Controls (VR401 & VR402) to their mechanical centers.
4. Set the G2 Screen Control (VR406) and the three Cut-Off Controls (VR403, VR404 & VR405) to minimum (fully CCW).
5. Slowly turn up the G2 Screen Control until the first faint color appears.
6. Slowly turn up the other two color Cut-Off Controls so as to match the first control setting.
7. Remove the ground from the R, G and B inputs and then adjust Red and Blue Drive Controls (VR401 & VR402) for a white screen.

NOTE: The schematic diagram for the Wells-Gardner in-line color monitor is supplied as part of this manual.

SECTION 6
TROUBLE SHOOTING GUIDE

6.1 IN CASE OF DIFFICULTY

The trouble shooting suggestions presented herein are not intended to be an all inclusive trouble shooting guide, but will serve to direct the technician to the most probably cause of difficulty.

SYMPTOM	MOST PROBABLE CAUSE
A. DEAD GAME	1. Open interlock (Front or Rear) Switch. 2. Blown Line Fuse (3A for 120 Vac line, 1.5A for 240 Vac line).
B. DEAD MONITOR	1. Blown monitor Fuse (3A, mounted on monitor). 2. Video Board unplugged from card rack, or cable disconnected between Video Board and monitor.
C. BAD OR MURKY COLOR	1. Degaussing of monitor bad. See paragraph 5.3. 2. Monitor in need of Purity Adjustment. See paragraph 5.4
D. "MULTIPLE" IMAGES IN DIFFERENT COLORS, ESPECIALLY NEAR EDGES OF MONITOR	1. Convergence adjustment of monitor is off. See paragraph 5.5.
E. NO VERTICAL HOLD, HORIZONTAL OKAY	1. Adjust vertical hold control on monitor. 2. Bad vertical counter or sync circuitry on Video Board. See paragraph 4.2.3 for detailed explanation of circuit operation.
G. BAD VERTICAL STRIPE OF VIDEO, UPPER OR LOWER HALF OF SCREEN, OTHER HALF GOOD	1. Bad RAM. RAMS 1B through 7B control upper half, 1C through 7C control lower half.
H. BAD HORIZONTAL BAR OR BARS OF VIDEO	1. Bad XOR gate or Adder on Video Board.
I. "GARBAGE" VIDEO, BUT SYNC OKAY	1. Reset game by grounding Pin 2 of 555 on Mother Board. 2. Check adjustment of +5 volt supply. Must be 5 volts at board, or +5.3 to +5.5 at power supply TP1.

I.	"GARBAGE" VIDEO, BUT SYNC OKAY (CONT'D)	3. Make sure all PROMS are plugged in. 4. Check +12 and -5 volt supplies on CPU Board. 5. Check Z-80 and Address and Data Bus Buffers. 6. Check CPU Board clock oscillator. 7. Check Scratch Pad Ram, CPU Board. 8. Check Read, Write & WAIT* State Logic Video Board. See paragraph 4.2.2 for detailed explanation of circuit operation.
J.	NO SOUND	1. Check +15V max.(VAUDIO) supply 2. Check Audio Power Amp (LM377) 3. Check Sound Enable 7407 and Output Port PIA.
K.	SOUND AFTER GAME OVER	1. Check Sound Enable 7407
L.	INDIVIDUAL SOUNDS MISSING	1. Check the individual control bit of the output PIA. 2. Check the 7407 open-collector buffer. 3. Check the Op-Amp(s) associated with the sound. 4. For the sounds that contain noise, check the noise generator shift register, and clock generator. 5. Check the +12 volt supply to I/O Sound Board.
M.	CREDIT INCREMENTS BUT NO COIN COUNTER ADVANCE	1. Check driver transistor on I/O Sound Board.
N.	NO CREDIT FROM COIN SWITCH, SERVICE SWITCH OKAY, COIN COUNTER OKAY.	1. Check Debounce one-shot (74LS123)
O.	PLAYER CANNOT MOVE IN ONE DIRECTION, OR CANNOT FIRE.	1. Check switch and associated wiring. 2. Check Debounce circuit. 3. Check Schmitt trigger. 4. Check input PIA (if game functions normally, and signal is at PIA, PIA should be replaced).
N.	PICTURE FLIPS BETWEEN PLAYERS ON UPRIGHT GAME.	1. Game has been straped for up-right operation. Remove strap located on I/O Sound Board and connect to inverter from out-put PIA.

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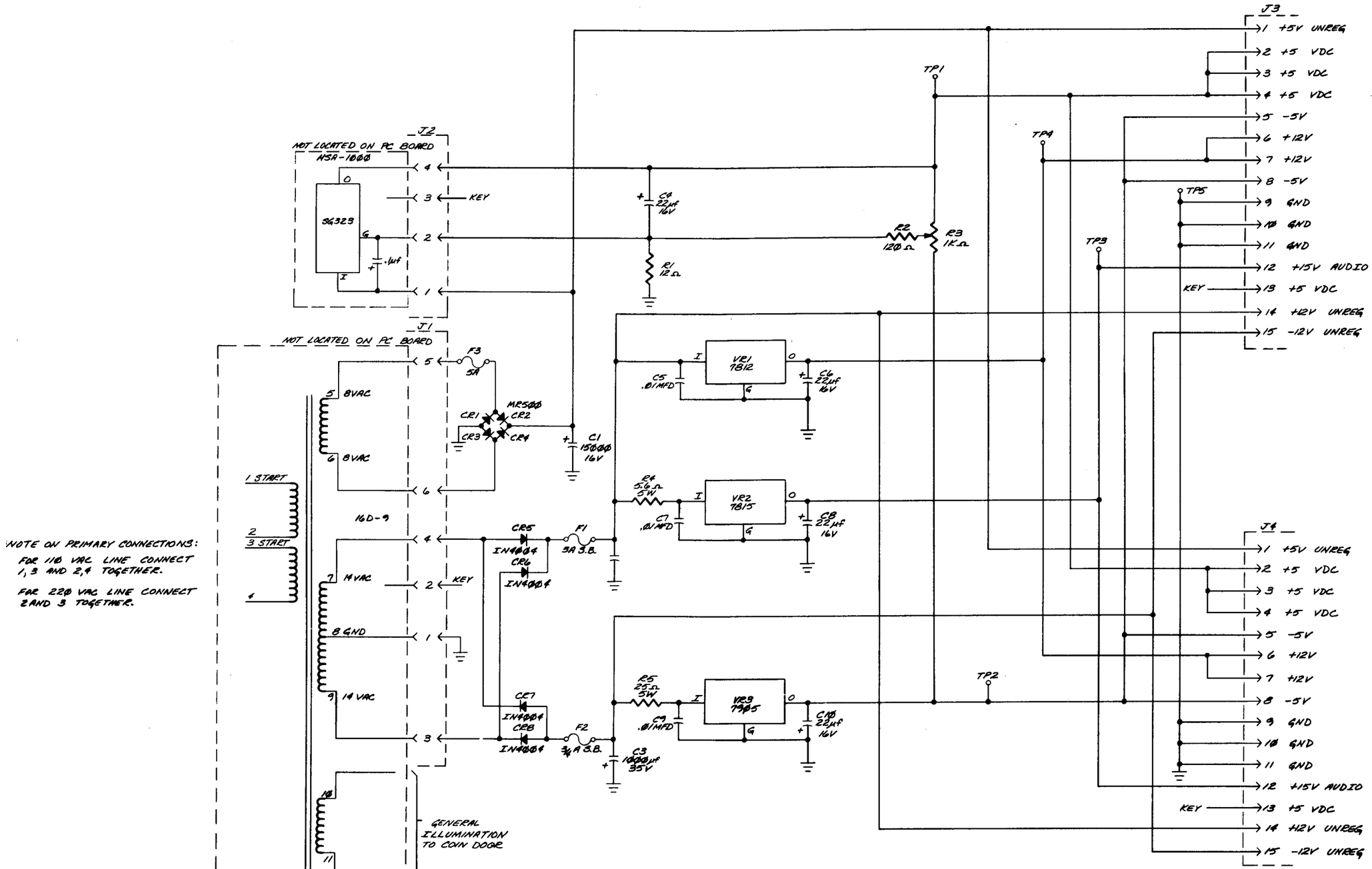

NOTE ON PRIMARY CONNECTIONS:

FOR 110 VAC LINE CONNECT 1, 3 AND 2, 4 TOGETHER.

FOR 220 VAC LINE CONNECT 2 AND 3 TOGETHER.

POWER SUPPLY
SCHEMATIC DIAGRAM

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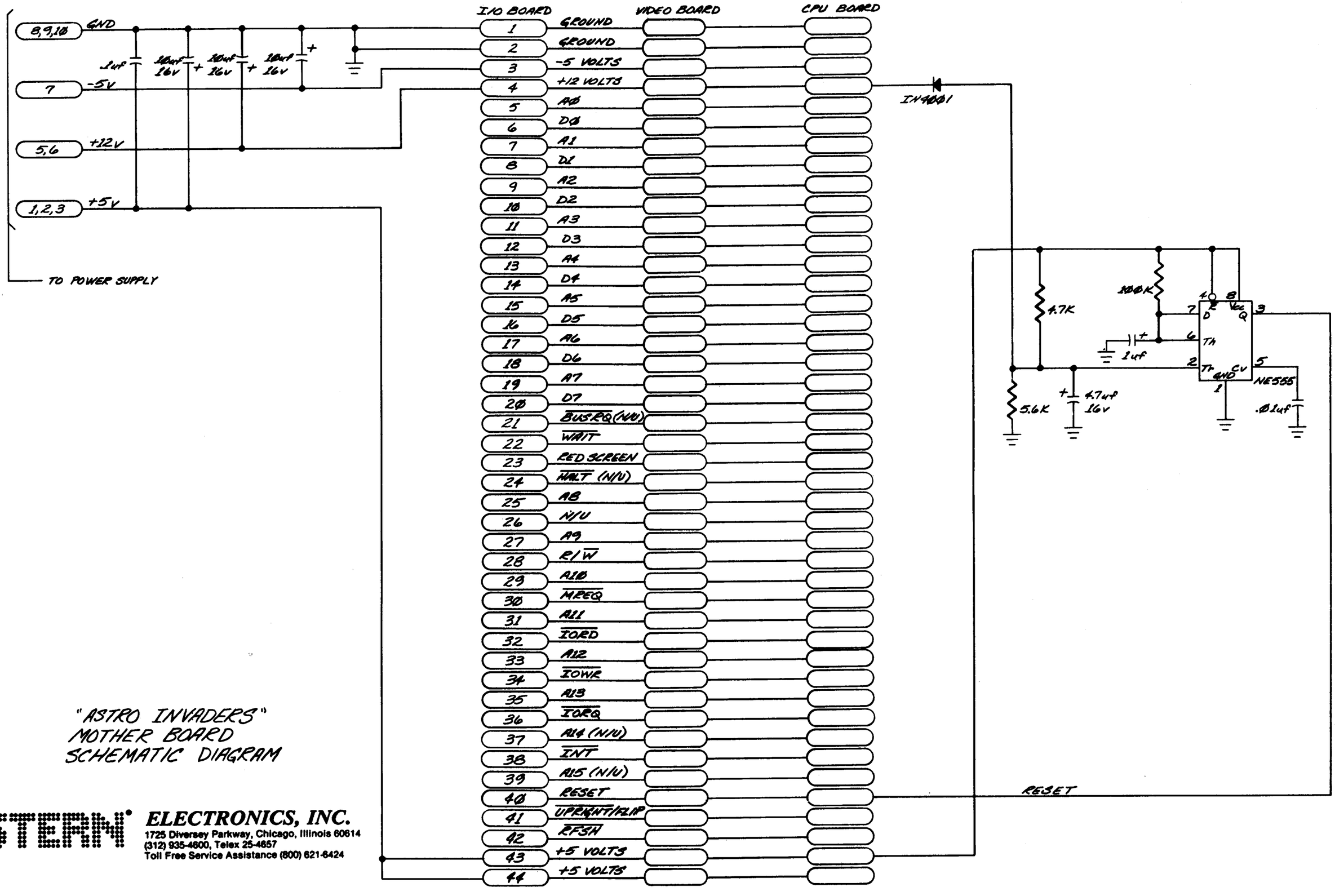

"ASTRO INVADERS"
MOTHER BOARD
SCHEMATIC DIAGRAM

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I/O SOUND BOARD
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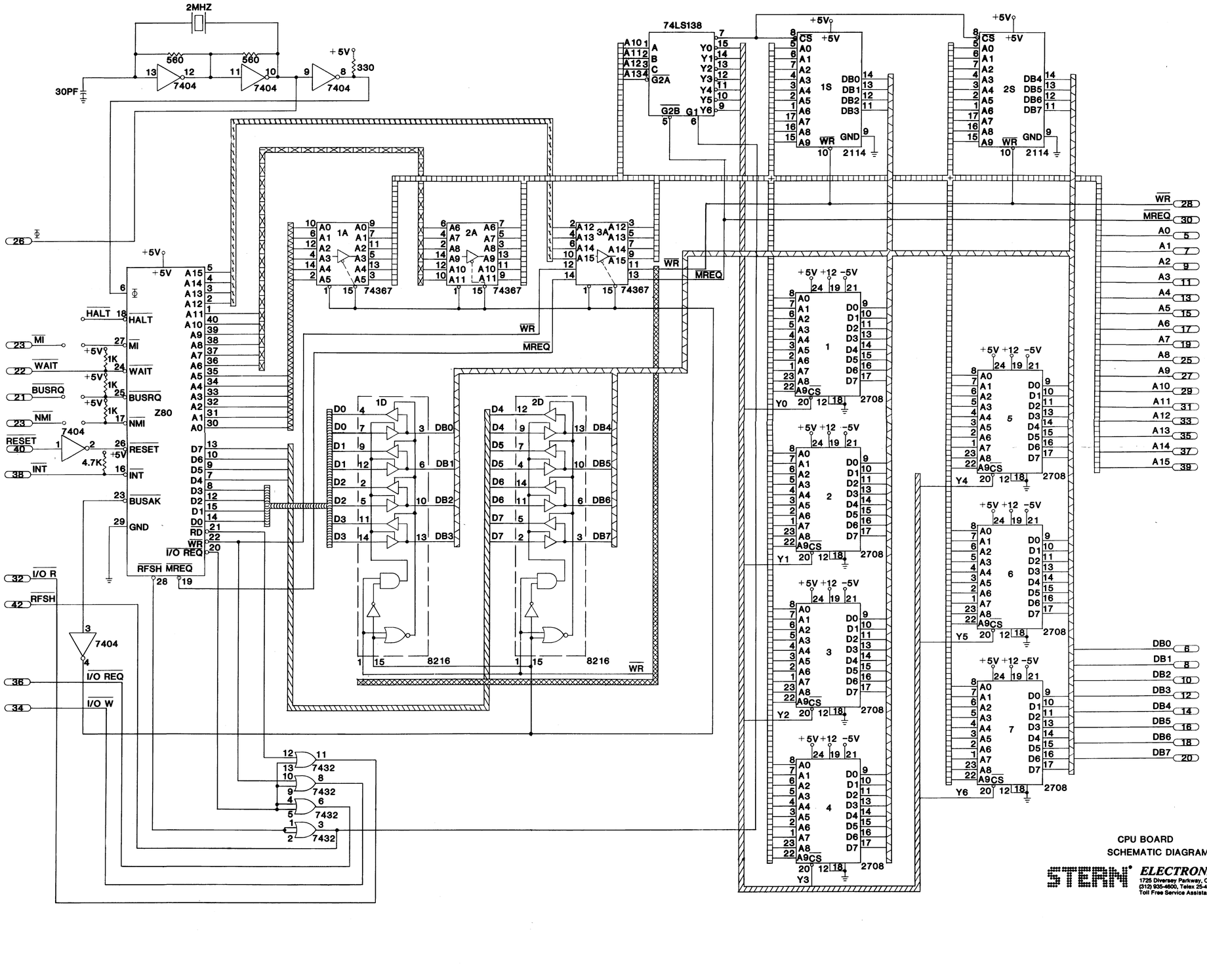

CPU BOARD
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CPU ADDRESS BUS

CPU DATA BUS

RAM ADDRESS BUS

RAM DATA OUT BUS

CPU RAM READ

CPU RAM WRITE

VIDEO ADDRESS BUS

PIXCLK

SHIFT/LOAD

BUS RQ

INT

COMPBLANK

SERIAL VIDEO

CPU RAM SELECT

TO MONITOR

CRT-RED

CRT-BLUE

CRT-GREEN

WAIT

R/W

RED SCREEN

VIDEO BOARD
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